Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 70071

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Third Semester

Computer Science and Engineering

CS 3351 — DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : B.E. Computer and Communication Engineering/B.Tech. Artificial Intelligence and Data Science/B.Tech. Computer Science and Business Systems/B.Tech. Information Technology)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the four possible elementary operations simple binary addition consists of.

2. What is a multiplexer?

3. Outline the difference between a synchronous sequential circuit and an asynchronous sequential circuit.

4. Define a latch and a flip-flop.

5. What are data transfer instructions?

6. Outline instruction cycle with a diagram.

7. What is a program counter?

8. Define pipelining.

9. What is hit time?

10. What is a direct-mapped cache?

PART B — (5 × 13 = 65 marks)

11. (a) Present the graphic symbol, algebraic expression and truth table for the following digital logic gates: AND, OR, Inverter, Buffer, NAND, NOR, Exclusive OR and Exclusive NOR. (13)

Or

(b) What is a K-map? Simplify the Boolean function $F(w, x, y, x) = \Sigma(0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$ using K-Map. (13)

12. (a) (i) What is an SR latch? Outline the design of SR latch using NOR gates. Also, present the function table for the same. (7)

(ii) Outline the design of a D flip-flop with two D latches and an inverter with a diagram. (6)

Or

(b) (i) Outline the Mealy model and Moore model of sequential circuits with a diagram. (6)

(ii) What is a shift register? Outline the design of a four-bit shift register with a diagram. (7)

13. (a) Outline the Von Neumann architecture with a diagram. (13)

Or

(b) What is an addressing mode? Outline the types of addressing mode with an example. (13)

14. (a) (i) Outline a control unit with a diagram and state the functions performed by a control unit. (8)

(ii) Outline the difference between hardwired control and micro programmed control. (5)

Or

(b) What are pipeline hazards? Outline the types of pipeline hazards. (13)

15. (a) Present an outline of virtual address, physical address, address translation, segmentation, page table, swap space and page fault. (13)

Or

(b) (i) Present an outline of interrupt driven I/O. (5)

(ii) Outline direct memory access with a diagram. (8)

PART C — (1 × 15 = 15 marks)

16. (a) Outline the design of a three to eight line decoder circuit using "inverters" and "AND" gates. Also, present the truth table for the same. (15)

Or

(b) Outline the design of a BCD ripple counter using JK flip-flops with state diagram and logic diagram. (15)

Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 30117

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2023.

Third Semester

Computer Science and Engineering

CS 3351 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to Computer and Communication Engineering/ Artificial Intelligence and Data Science/Computer Science and Business Systems/Information Technology)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Construct Half-adder and full adder circuits.
2. Evaluate the logic circuit of 2 bit comparator.
3. Distinguish sequential logic with combinational logic.
4. Give the excitation table of JK flip flop.
5. Draw the stock diagram of Von-Neumann architecture.
6. List the types of addressing modes.
7. What do you mean by pipelining? List its types.
8. Differentiate data hazards and control hazards.
9. Why do we need cache memory?
10. Which signal is used to notify the processor that the transfer is completed? Define.

PART B — (5 × 13 = 65 marks)

11. (a) (i) How will you design a full adder using two half adders. (7)

(ii) Simplify the function using multiplexer $f = \Sigma(0, 1, 3, 4, 8, 9, 15)$. (6)

Or

(b) (i) Demonstrate 4 bit magnitude comparator with three outputs $A > B$, $A = B$, $A < B$. (7)

(ii) Build a 4 bit priority encoder using gates. (6)

12. (a) (i) Realize D flip flop using SR flip flop. (7)

(ii) Construct a 4 bit down counter using logic gates. (6)

Or

(b) Give the analysis and design of clocked sequential circuits.

13. (a) (i) Explain about functional units in digital computer. (7)

(ii) Discuss about instruction cycle. (6)

Or

(b) (i) Explain about encoding in assembly language and types of instructions. (7)

(ii) Discuss the interaction between assembly language and high level language. (6)

14. (a) An instruction pipeline has five stages where each stage takes 2 nanoseconds and all instructions use all five stages, branch instruction are not overlapped (i.e.) the instruction after the branch is not fetched till the branch instruction is completed. Under ideal condition.

Calculate the average instruction execution time assuming that 20% of all instruction executed are branch instructions. Ignore the fact that some branch instructions may be conditional.

Or

(b) (i) What is hazard? Give hazard free realization for the following Boolean function $F(A, B, C, D) = \Sigma m(1, 5, 6, 7)$ using AND-OR gate network. (10)

(ii) Define essential hazards. (3)

15. (a) (i) Explain in detail about DMA operation. (7)

(ii) Give the modes of DMA transfer. (6)

Or

(b) Elucidate interconnection standards. (13)

PART C — (1 × 15 = 15 marks)

16. (a) Explain the functions with the state diagram and characteristic equation of T, D and JK flip flop. Compare and Contrast. (15)

Or

(b) Implement the following Boolean function using 8 × 1 multiplexer. Considering D as the input and A, B, C as selection lines

$f(A, B, C, D) = AB' + BD + B'CD'$. (15)

Reg. No. : | E | N | G | G | T | R | E | E | . | C | O | M |

Question Paper Code : 20864

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023

Third Semester

Computer Science and Engineering

CS 3351 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design / Computer Science and Engineering (Artificial Intelligence and Machine Learning) / Computer Science and Engineering (Cyber Security) / Computer and Communication Engineering / Artificial Intelligence and Data Science / Computer Science and Business Systems and Information Technology)

(Regulations 2021)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Write down the sum and carry expressions for half adder.
2. How many selection inputs, data inputs and output for 16 X 1 MUX?
3. What is shift register? List its types.
4. How many flip flops are required for designing BCD counter? Justify.
5. List the functional units of a digital computer.
6. Interpret the Instruction Set Architecture.
7. What is program counter?
8. When do data hazards occur in pipelining?
9. What is memory hierarchy?
10. Differentiate write back and write through.

PART B — (5 × 13 = 65 marks)

11. (a) Explain full adder and full subtractor with the help of circuit diagrams.

Or

(b) Explain binary to octal decoder and octal to binary encoder with the help of circuit diagrams.

12. (a) Describe J-K and D flip flops with the help of block diagrams and characteristic tables.

Or

(b) Explain Mealy and Moore Models with the help of block diagrams.

13. (a) Explain about any four addressing modes with example.

Or

(b) Describe Instruction sequencing and branching with examples.

14. (a) Depict how instruction is being fetched and executed through the data path in the processor?

Or

(b) Describe data hazards and control hazards. Explain with suitable techniques, how these hazards can be mitigated?

15. (a) Explain how memory mapping techniques are useful for finding the memory blocks in cache?

Or

(b) How virtual addresses are translated into physical addresses? Explain it with the help of virtual memory organization and page translation.

PART C — (1 × 15 = 15 marks)

16. (a) Using K – Map, find the sum of products and product of sums for the given function $F = \sum_m (0,2,6,7,8,10,12,14,15)$.

Or

(b) Design a Mod – 7 synchronous counter using J – K flip flop.

Reg. No. : E N G G T R E E . C O M

Question Paper Code : 50897

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024

Third Semester

Computer Science and Engineering

CS 3351 – DIGITAL PRINCIPLES AND COMPUTER ORGANIZATION

(Common to : Computer Science and Design / Computer Science and Engineering (Artificial Intelligence and Machine Learning) / Computer Science and Engineering (Cyber Security) / Computer and Communication Engineering / Artificial Intelligence and Data Science / Computer Science and Business Systems / Information Technology)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is combinational circuit?
2. Which combinational circuit is otherwise known as data selector? Why?
3. Write down the characteristic table of T flip flop.
4. Compare Mealy and Moore Models.
5. What is the difference between register addressing mode and register indirect addressing mode?
6. What is data transfer instruction? Specify any two data transfer instructions.
7. What is pipelining?
8. Differentiate: Hardwired Control and Microprogrammed Control.
9. Can a computer work without cache? Justify.
10. What is the purpose of SATA?

PART B — (5 × 13 = 65 marks)

11. (a) Why do we need a code conversion? Explain with the conversion of binary to gray code.

Or

(b) Identify the combinational circuit that is used to compare the relative magnitude of two binary numbers. Construct the identified circuit for comparing 2-bit binary numbers.

12. (a) Which flip flop is called as data flip flop? Explain the operation of the same with its circuit diagram, characteristic table and excitation table.

Or

(b) Which counter is called decade counter? Why? Explain the operation of the same in asynchronous mode.

13. (a) Explain Von Neumann Architecture with neat sketch.

Or

(b) Describe any five addressing modes with examples.

14. (a) Draw a simple MIPS data path with control unit and explain the execution of ALU instruction.

Or

(b) Describe the methods for avoiding the control hazards.

15. (a) Explain in detail the memory hierarchy with neat diagram.

Or

(b) Explain in detail about Direct Memory Access (DMA) with neat diagram.

PART C — (1 × 15 = 15 marks)

16. (a) Design a Mod-5 Synchronous Counter using JK flip flop.

Or

(b) Design 8 × 1 MUX. Implement the following Boolean function using 8 × 1 MUX $F(P,Q,R,S) = \sum m(0,1,3,4,8,9,15)$.