MUTHAYAMMAL ENGINEERING COLLEGE

(An Autonomous Institution)

(Approved by AICTE, New Delhi, Accredited by NAAC & Affiliated to Anna University)
Rasipuram - 637 408, Namakkal Dist., Tamil Nadu.

Estd. 2000

Department of Electronics and Communication Engineering
Question Bank - Academic Year (2021-22)

Course Code & Course Name : 19ECC04& Digital System Design

Name of the Faculty : Dr.P.Padmaloshani

Year/Sem/Sec : II / III/A

UNIT-I: BASIC CONCEPTS OF DIGITAL SYSTEMS AND LOGIC FAMILIES

Part-A (2 Marks)

1. Prove that x + xy = x.
2. Simplify the following Boolean expression:
   $XY + \overline{X}Z + YZ$
3. Given the two binary numbers X = 1010100 and Y = 1000011, perform the subtraction Y - X using 2s complements.
4. Which gates are called as the universal gates? What are its advantages?
5. What is prime implicant?
6. State Duality principle.
7. State De-Morgan's theorem and mention its use.
8. List out the advantages and disadvantages of K-map method.
9. What are the types of logic families?
10. Convert Y=A+BC'+AB+A'BC into canonical form.

Part-B (16 Marks)

1. (i) State the postulates of Boolean algebra. (8)

   (ii) Find a Min SOP for f = b'c'd + bcd + acd' + a'b'c + a'bc'd. (8)

2. Find an expression for the following function using Quine McCluscky method F= ∑m (0, 2, 3,5,7,9,11,13,14,16,18,24,26,28,30) and Draw the logical circuit of the minimal expression. (16)

3. (i) Find the F(A, B,C,D) = ∑m(1,4,6,10) + ∑d (0,11) using K-Map method and Draw the logical circuit of the minimal expression. (8)

   (ii) Explain the working of 2 input TTL totem-pole NAND gate circuit. (8)

4. Simplify the Boolean function F(A, B,C,D) = ∏ M (1,3,7,11,15) + ∏d (0,2,5) .if don't care conditions are not taken care, What is the simplified Boolean function .What are your comments on it? Implement both circuits. (16)

5. Simplify the following function using tabulation method Y(a.b,c,d) = ∑m (16)

$(0,1,2,5,6,8,9,10) + \sum d(7,14)$ and implement logical gates.

UNIT-II : COMBINATIONAL CIRCUITS

Part-A (2 Marks)

1. Define Combinational circuit.
2. Design procedure for combinational circuits.
3. Draw the block diagram of half adder. Write truth table and draw logic diagram.
4. Draw the block diagram of half subtractor. Write truth table and draw logic diagram.
5. Illustrate 4-bit Binary parallel adder?
6. What do you mean by comparator?
7. Write the truth table of 4:1 multiplexer.
8. Application for parity checker and parity generator.
9. What do you mean by carry propagation?
10. Difference between decoder and demux.

Part-B (16 Marks)

1. (i) Design a 3-bit magnitude comparator. (8)

   (ii) Explain the concepts of carry look ahead adder with neat logic diagram. (16) (8)

2. (i) Realize a BCD to Excess 3 code conversion circuit starting from its truth table. (8)

   (ii) Design a full Adder using 2-half adder. (8)

3. (i) Design a 1X4 De-multiplexer circuit. (8)

   (ii) Implement the following Boolean function $F= \sum m (0,3,5,8,9,10,12,14)$. Using 8:1 Mux. (8)

4. (i) Explain in detail about parity generator and parity checker. (8)

   (ii) Translates from Excess 3 to BCD 8421 code. (8)

5. (i) Explain Decimal to BCD encoder with neat logic diagram. (8)

   (ii) Design and explain a 1 of 8 demultiplexer. (8)

UNIT-III : SEQUENTIAL CIRCUITS

Part-A (2 Marks)

1. Give the comparison between combinational circuits and sequential circuits.
2. Define race around condition in flip flop.
3. Write the excitation table for SR FF.
4. How does a JK flip flop differ from the SR flip flop in its basic operation?
5. Outline the uses of ring counter.

6. Write the characteristic equation of JK FF.
7. How the lock-out condition can be avoided?
8. How many filp flops are needed for a mod 60 counter?
9. What is shift register? and its types.
10. What is edge triggered flip flop?

Part-B (16 Marks)

1.(i) Write the characteristic table and characteristic equation of SR and D flip flop. (8)

(ii) Explain the characteristic table and characteristic equation of JK and T flip flop. (8)

2.(i) Explain the working of BCD Ripple Counter with the help of state diagram and logic diagram. (8)

(ii) Design mod-10 synchronous counter using JK Flip Flops. (8)

3.(i) Explain the shift registers and its types. (8)

(ii) Explain the universal shift registers. (8)

4.(i) With neat diagram explain master / slave JK-flip flops. (8)

(ii) Summarize the design procedure for Synchronous Sequential circuit. (8)

5.(i) Design a Ring counter and explain in detail. (8)

(ii) Design a Johnson counter and explain in detail. (8)

UNIT-IV : SYNCHRONOUS AND ASYNCHRONOUS SEQUENTIAL CIRCUITS

Part-A (2 Marks)

1. Distinguish between synchronous sequential circuits asynchronous sequential circuits.
2. Distinguish Mealy and Moore models?
3. Define state assignment
4. Short notes on state reduction.
5. What is meant by excitation table?
6. State the types of sequential circuits.
7. What is meant by Race?
8. Distinguish between fundamental mode and pulse mode operation of asynchronous sequential circuits.
9. What do you mean by Hazards? and give its types.
10. How to eliminate the hazard?

Part-B (16 Marks)

1.(i) An asynchronous sequential circuit is described by the following excitation and function $X=(Y_1Z_1'W2)X+(Y_1'Z_1W_2')$ $S=X'$ (8)

(a) Draw the logic diagram of the circuit (b) Derive the transition table & output map

(c) Describe the behavior of the circuit.

(ii) Explain the fundamental & pulse mod asynchronous sequential circuit. (8)

2.(i) Explain Essential, Static and Dynamic hazards in digital circuit. Given Hazards free realization for following Boolean function. $F(I, J, K,L)=\Sigma(1,3,4,5,6,7,9,11,15)$ (8)

(ii) Explain in detail Race Free State assignment. (8)

3.(i) Summarize the design procedure for asynchronous sequential circuit. (8)

(ii) Give examples for critical race & cycle and explain. (8)

4.(i) Write short notes on hazards and its types. (8)

(ii) What is the objective of state assignment in asynchronous circuit? Give hazard – free realization for the following Boolean function $f(A, B,C,D) = M(0,2,6,7,8,10,12)$ (8)

5.(i) Design a synchronous sequential sequence 0,1,2,3,4,5,6,0. (8)

(ii) Explain Hazards free combinational circuits. (8)

UNIT-V: PROGRAMMABLE LOGIC DEVICES MEMORY AND VHDL

Part-A (2 Marks)

Memories: ROM, PROM, EPROM, PLA, PLD, FPGA – VHDL Programming: RTL Design – Combinational Logic – Types – Operators – Packages – Sequential Circuits – Sub Programs – Testbenches. (Examples: adders, counters, flip flops, FSM, Multiplexers / De-Multiplexers).

1. List the advantages of PROM and EPROM
2. Compare and contrast EEPROM and flash memory.
3. What is mean by PLDs?
4. Mention the applications of PLA.
5. List the applications of PAL.
6. Point out the applications of FPGA.
7. Differentiate between PAL and PLA.
8. How does ROM retain information?
9. Write the advantages of PROM and EPROM
10. How does the architecture of a PLA different from the PROM?

Part-B (16 Marks)

1. (i) Implement the following functions using PLA (8)

$F1(x,y,z) = \sum m(1,2,4,6)$, $F2(x,y,z) = \sum m(0,1,6,7)$, $F3(x,y,z) = \sum m(2,6)$

(ii) Explain the Architecture of FPGA. (8)

2. Implement the following Boolean functions using PAL (16)

$W(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13)$

$X(A,B,C,D) = \sum m(0,2,6,7,8,9,12,13,14)$

$Y(A,B,C,D) = \sum m(2,3,8,9,10,12,13)$

$Z(A,B,C,D) = \sum m(1,3,4,6,9,12,14)$

3. Design a BCD to Excess-3 code converter and implement using suitable PLA. (16)

4. (i) Explain the organization of ROM with relevant diagrams. (8)

(ii) Write note on PAL. (8)

5. (i) Explain the structures of PLA and PAL (8)

(ii) Design ROM for the following functions F1 = $\sum$ (1,2,3) ; F2 = $\sum$ (0,2) (8)

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