Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 50968

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2024.

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is threshold voltage of MOS transistor?
2. Show how nMOSFET acts as a switch?
3. What is stick diagram? Draw the stick diagram for two input NAND gate.
4. Realize the two input NAND gate using pass transistor logic.
5. Differentiate latches and registers.
6. What is clock skew? How to overcome clock skew?
7. Find the propagation delay of n-bit carry select adder.
8. Write the logic equation for the 3-bit magnitude comparator.
9. List the issues in testing microchip design process.
10. What are the different types of ASICs?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Obtain the drain current in three different regions of operation. (7)

(ii) Show how channel length modulation affects the drain current and body effect affects the threshold voltage? (6)

Or

(b) What is the dynamic condition of MOSFET? Discuss the transistor characteristics of MOSFET under dynamic conditions. (13)

12. (a) (i) Find the Elmore's constant of the 4-input NAND gate. (7)

(ii) Realize the 4:2 encoder using CMOS logic. (6)

Or

(b) (i) Explain the concept of dynamic logic. Realize the 3-input NAND gate using dynamic logic. (7)

(ii) Describe the disadvantages of dynamic logic. Provide the solution to overcome the dynamic logic. (6)

13. (a) Elucidate the static latches and registers suitable for sequential logic circuit design. (13)

Or

(b) (i) Draw the monostable multivibrator using CMOS transistor and explain the operation. (7)

(ii) What are the timing classification of digital systems? Show how the timing is applied for synchronous design. (6)

14. (a) (i) What is the need for carry save adder? Explain the 4-bit carry save adder. (6)

(ii) What is an array multiplier? Show how array multiplier uses an array of cells for computing the result. (7)

Or

(b) Illustrate the hierarchical memory architecture and explain the building blocks of memory architecture. (13)

15. (a) (i) What are the faults in ASIC design? Model the faults in ASIC design. (7)

(ii) Explain the design flow process suitable for ASIC. (6)

Or

(b) (i) Write the test bench in Verilog HDL for a combinational circuit. (6)

(ii) Explain the test interface and boundary scan suitable for scan design. (7)

PART C — (1 × 15 = 15 marks)

16. (a) (i) What is pipelining? Apply the pipelining concept and find the total clock time required for obtaining outputs for $y = |a_n + b_n|$ where $n = 1, 2, 3, 4, 5$. (7)

(ii) Realize the function $F = \Sigma m(1, 5, 6, 7)$ using (8)

(1) Pseudo nMOS logic

(2) Static CMOS logic.

Or

(b) (i) Generate the test vectors for the combinational function F = (AB + BC + CD) using automatic test pattern generation for the stuck-at-0 fault at node B. (8)

(ii) Realize the functions $F_1 = X_0 X_1 + X_1' X_2'$; $F_2 = X_0' X_1' + X_1 X_2$ sing programmable logic array. (7)

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20935

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Fifth Semester

Electronics and Communication Engineering

EC 3552 – VLSI AND CHIP DESIGN

(Common to : Electronics and Telecommunication Engineering)

(Regulations 2021)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. How does MOSFET act as a switch?

2. Realize the 2:1 multiplexer using transmission gates.

3. Draw the stick diagram for 2-input NAND gate.

4. What are the disadvantages of pass transistor logic?

5. Differentiate latches and registers.

6. What are the timing classification of digital system?

7. List the various interconnect parameters analyzed in VLSI chip design.

8. What is the significance of FPGA?

9. Differentiate FPGA design and ASIC design flow.

10. Write the test bench in Verilog HDL to test the D-flip flop.

PART B — (5 × 13 = 65 marks)

11. (a) (i) Obtain the first order model relating the current and voltage (I-V) for an nMOS transistor in three regions of operation. (7)

(ii) Discuss the velocity saturation and mobility degradation of an nMOS transistor under non-ideal I-V effects. (6)

Or

(b) Elucidate the dynamic behaviour of MOSFET and discuss each of the component. (13)

12. (a) (i) Realize the AND gate using pass transistor logic and explain the operation circuit. (6)

(ii) Discuss the disadvantages of dynamic logic gates. Provide the solution to overcome the disadvantages. (7)

Or

(b) (i) Find the Elmore's constant for 4-input NAND gate. (6)

(ii) What are the types of power dissipation in CMOS circuits? Find the total power dissipation and discuss the low power design principles. (7)

13. (a) (i) Explain the multiplexer based latches and master slave edge triggered register. (7)

(ii) Describe the true single phase clock register. (6)

Or

(b) (i) Illustrate the combined effect of skew and jitter in sequential logic circuit and find the time period of the clock. (7)

(ii) Design the sequential logic circuit based on self-timed approach. (6)

14. (a) (i) Write the design techniques in dealing with capacitive cross talk. (6)

(ii) Describe the design techniques available to the designer to address the voltage drop over the inductor problem. (7)

Or

(b) (i) Realize the combinational function with PLA.

$$Y1 = \sum m(2,3,4,6) \qquad Y2 = \sum m(1,2,3,4)$$ (7)

(ii) Elucidate the basic architecture of FPGA. (6)

15. (a) (i) Illustrate the microchip design process and identify the issues in test. (7)

(ii) What are common fault models in CMOS design? With a suitable diagram enlighten the causes of faults. (6)

Or

(b) (i) Explain the automatic test pattern generation with a suitable example. (7)

(ii) Describe the boundary scan with necessary diagrams. (6)

PART C — (1 × 15 = 15 marks)

16. (a) Realize the sum of minterms $F = \sum m(0,1,7,11,15) + \sum d(2,3,5)$ using

(i) Static CMOS logic and (7)

(ii) Clocked CMOS logic. (8)

Or

(b) (i) Apply the concept of 3-stage pipelining to $\log(|a_n + b_n|)$ and find the number clock period for $n=3$ to get the output. (7)

(ii) Design a 4-bit binary to excess-3 code converter using ROM. (8)

———————

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work

Reg. No. | | | | | | | | | | | | |

Question Paper Code : X10348

B.E./B.Tech. DEGREE EXAMINATIONS NOVEMBER/ DECEMBER 2020 AND APRIL / MAY 2021

Sixth /Seventh Semester

Electronics and Communication Engineering

EC8095- VLSI DESIGN

(Common to: Electronics and Telecommunication Engineering/ Electrical and Electronics Engineering/ Electronics and Instrumentation Engineering)

(Regulations 2017)

Time: 3 Hours | Answer ALL Questions | Max. Marks 100

PART- A (10 x 2 = 20 Marks)

1. Sketch a complementary CMOS gate computing Y = (AB + BC)′.
2. What is body effect?
3. What is the logical effort for two input NOR gate? (Assume the required values)
4. What is the use of transmission gates?
5. List the timing classification of Digital system.
6. Differentiate latches and flip-flops.
7. Draw the dot diagram for Wallace tree multiplier.
8. List the categories of memory arrays.
9. What is the significance of field programmable gate arrays?
10. Identify the ways to optimize the manufacturability, to increase yield.

PART- B (5 x 13 = 65 Marks)

11. a) i) Differentiate static and dynamic latches and registers. **6**

ii) Obtain the first-order model relating the current and voltage for an nMOS transistor in three regions of MOS operation. **7**

OR

b) i) Explain the DC transfer characteristics of CMOS inverter. **6**

ii) Estimate the delay of CMOS logic gates as the RC product of the effective driver resistance and the load capacitance. **7**

12. a) Sketch a combinational function Y = (A(B+C+D)+ E.F.G)′ using

i. Pseudo-nMOS logic **4**

ii. Domino logic **4**

iii. Cascode voltage switch logic. **5**

OR

b) Explain the pass transistor logic and show how complementary pass transistor logic and double pass transistor logic are applied for 2: 1 multiplexer. **13**

13.	a)	i. Illustrate the circuit designs for basic latches, then build the flip-flops and pulsed latches.	**7**
		ii. Design the pulse registers suitable for sequential CMOS circuits.	**6**
		OR	
	b)	i) Describe the concept of pipelining in sequential circuits with a suitable example.	**7**
		ii) Sketch and explain the Monostable sequential circuits based on CMOS logic.	**6**
14.	a)	i) Explain the carry-propagate adder and show how the generation and propagation signals are framed.	**6**
		ii) List the several commonly used shifters. Design the shifter that can perform all the commonly used shifters.	**7**
		OR	
	b)	Illustrate the building blocks of Memory architectures and memory peripheral circuitry adapted to operate for non-volatile memory.	**13**
15.	a)	i) Show how routing is performed in FPGA interconnect.	**6**
		ii) Illustrate the basic building block architectures of FPGA.	**7**
		OR	
	b)	Explain the three main approaches commonly used for design for testability (DFT).	**13**

PART- C (1 x 15 = 15 Marks)

16.	a)	i) Differentiate static and dynamic power in CMOS circuits.	**7**
		ii) Sketch the 4:1 multiplexer using transmission gates.	**8**
		OR	
	b)	Generate the partial products using radix-4 booth encoded multiplier to compute 01110_2 x 01101_2. For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier.	**15**

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 20457

B.E./B.Tech. DEGREE EXAMINATIONS, APRIL/MAY 2022.

Sixth/Seventh Semester

Electrical and Electronics Engineering

EC 8095 — VLSI DESIGN

(Common to : Electronics and Communication Engineering / Electronics and Instrumentation Engineering / Electronics and Telecommunication Engineering / Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Sketch a complementary CMOS gate computing W=(XY+YZ)'
2. Write the expression for parasitic delay & logical effort of an N-input NAND gate.
3. What is the use of transmission gates?
4. List the sources of power dissipation in CMOS circuits.
5. What is meant by bistability?
6. Define clock-skew and clock-jitter.
7. Draw the circuit diagram of 1-bit binary shifter using MOS transistor.
8. State the need of sense amplifier in a memory cell.
9. What is the significance of field programmable gate arrays?
10. What are limitations of IDDQ testing?

PART B — (5 × 13 = 65 marks)

11. (a) (i) Explain the DC transfer characteristics of CMOS inverter. (6)

(ii) Estimate the delay of CMOS logic gates as the RC product of the effective driver resistance and the load capacitance. (7)

Or

(b) Write the layout design rules and draw the diagram for 4 input NAND and NOR gates.

12. (a) Explain pass transistor logic and show how complementary pass transistor logic and double pass transistor logic applied for 2:1 MUX.

Or

(b) Sketch a combinational function $Y = (AB + CD)'$.

(i) Pseudo-nMOS logic (4)

(ii) Domino logic (4)

(iii) Cascode voltage switch logic. (5)

13. (a) Explain the circuit and working of CMOS implementation of Schmitt trigger.

Or

(b) (i) Describe the concept of pipelining in sequential circuits with suitable example. (7)

(ii) Sketch and explain monostable sequential circuits based on CMOS logic. (6)

14. (a) (i) Explain the concept of carry look-ahead adder with neat diagram. (9)

(ii) Discuss trade-off between speed Vs area. (4)

Or

(b) Elucidate in detail the design of low power SRAM memory circuits.

15. (a) Describe FPGA interconnect routing resources with neat diagram.

Or

(b) Explain three main approaches commonly used for Design for Testability (DFT).

PART C — (1 × 15 = 15 marks)

16. (a) Realize a 2-input EXOR using static CMOS, transmission gate and dynamic CMOS logic. Analyze the hardware complexity.

Or

(b) Apply radix-2 encoding to realize a 4 big signed multiplier for $(-11)\times(-12)$. For the same multiplier apply radix-8 booth encoding and justify the advantages between radix-4 and radix-8 booth multiplier.

---

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 90460

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2022.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 – VLSI DESIGN

(Common to : Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw a 2-input CMOS NOR gate.

2. By what factor R_{DS} should be scaled, if constant electric field scaling is employed?

3. Using transmission gate draw a 4:1 MUX.

4. What is charge sharing in dynamic CMOS logic?

5. State the use of Schmitt Trigger.

6. Draw a MUX based negative level sensitive D-latch.

7. Compare SRAM and DRAM.

8. Draw a 1-transistor DRAM cell.

9. Define controllability and observability.

10. Mention the advantages of BIST.

PART B — (5 × 13 = 65 marks)

11. (a) With neat diagram, enumerate in detail the DC characteristics of CMOS inverter. (13)

Or

(b) (i) Analyze the switching characteristics of a CMOS inverter. Derive rise time, fall time and propagation delay. (6)

(ii) If two CMOS inverters are cascaded with an aspect ratio of 1:1 then determine the inverter-pair delay. (7)

12. (a) (i) Design a half adder using static CMOS logic. (6)

(ii) Design a 4:1 MUX using 2:1 MUX. Realize it using transmission gate. (7)

Or

(b) Realize a 2-input NOR gate using static CMOS logic, Domino logic and Complementary pass transistor logic. Analyze the hardware complexity in terms of transistor count. (13)

13. (a) (i) Enumerate in detail on the design of pulse registers. (6)

(ii) Give in detail, the design and working of astable sequential circuits. (7)

Or

(b) (i) Design a master-slave positive edge triggered D-flipflop using transmission gate. (6)

(ii) Discuss on sense amplifier based registers. (7)

14. (a) Describe the hardware architecture of a 4-bit signed array multiplier. (13)

Or

(b) (i) Elaborate in detail the design of a 4-bit barrel shifter. (6)

(ii) Describe the working of 6-transistor SRAM cell. (7)

15. (a) Explain in detail the basic architecture of FPGA with a neat diagram. (13)

Or

(b) Enumerate in detail the working of

(i) Adhoc Test (5)

(ii) Scan based Test (8)

PART C — (1 × 15 = 15 marks)

16. (a) Apply Radix-2 booth encoding to perform multiplication between two 8-bit numbers (-5) and 4. (15)

Or

(b) (i) Design a 4-bit carry look ahead adder using dynamic CMOS logic by deriving the necessary expressions. (6)

(ii) Design a 3-bit even parity generator using NAND gates only. Design the circuit using static CMOS logic. (9)

———————

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 70499

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2023.

Sixth/Seventh Semester

Electronics and Communication Engineering

EC 8095 — VLSI DESIGN

(Common to : Electrical and Electronics Engineering/Electronics and Instrumentation Engineering/Electronics and Telecommunication Engineering/Instrumentation and Control Engineering/Robotics and Automation)

(Regulations 2017)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw the stick diagram of a 3-input NAND gate.
2. Sketch the RC equivalent circuit of a CMOS inverter.
3. Obtain the logical efforts of footed and unfooted domino buffers.
4. What are the sources for gate leakage current in CMOS circuits?
5. State the applications of sense amplifier circuits.
6. Compare the data path for computation of $\log(|a+b|)$ in pipelined and non-pipelined design.
7. Draw the circuit schematic of a mirror adder circuit and mention its significance.
8. Sketch the block diagram of a 4 × 4 multiplier and highlight one possible critical path.
9. How is IDDQ testing performed?
10. List the building blocks of FPGA.

PART B — (5 × 13 = 65 marks)

11. (a) What are the non-ideal effects on I-V characteristics? Obtain the expression for critical electric field including the non-ideal effects.

Or

(b) Obtain the expression for long channel drain current in cutoff, linear and saturation regions.

12. (a) Sketch HI-skew and LO-skew 3-input NAND gate. Determine the logical effort of each gate during its transition.

Or

(b) Elaborate on the sources of static power dissipation in CMOS devices.

13. (a) Discuss the working of pulse registers using

(i) Glitch generation logic (7)

(ii) Flow-through register (6)

Or

(b) Establish the property "*A C²MOS – based pipeline circuit is race free as long as all the logic functions F between the latches are non-inverting*" using suitable circuit.

14. (a) Design a full adder cell using transmission gates. Use Manchester carry gates to obtain propagate and generate terms of the adder.

Or

(b) Discuss the working of a basic differential sense amplifier circuit. How differential sensing is applied to an SRAM memory column?

15. (a) Explain the parallel scan based testing procedure. List its advantages over serial scan chains.

Or

(b) Elaborate on the role played by pseudo-random sequence generator during execution of BIST.

PART C — (1 × 15 = 15 marks)

16. (a) Sketch a 3-input symmetric NOR gate. Size the inverters so that the pull-down is four times as strong as the net worst-case pull-up. Label the transistor widths. Estimate the rising, falling, and average logical efforts. How do they compare to a static CMOS 3-input NOR gate?

Or

(b) When adding two unsigned numbers, a carry-out of the final stage indicates an overflow. When adding two signed numbers in two's complement format, overflow detection is slightly more complex. Develop a Boolean equation for overflow as a function of the most significant bits of the two inputs and the output.

———————

www.Poriyaan.in

ECE - Department

ANNA UNIVERSITY – 2021 Regulation

Anna University ECE - Reg 2021

1st Semester

- Professionsal English I
- Matrices and Calculas
- Engineering Physics
- Engineering Chemistry
- Problem Solving & Python Programming

2nd Semester

- Professional English II
- Statistics and Numerical Methods
- Engineering Graphics
- Physics for Electronics Engineering
- Electrical and Instrumentation Engineering
- Circuit Analysis

3rd Semester

- Random Process & Linear Algebra
- C Programming & Data Structures
- Signals and Systems
- Electronic Devices and Circuits
- Control Systems
- Digital Systems Designs

4th Semester

- Electromagnetic Fields
- Networks & Security
- Linear Integrated Circuits
- Digital Signal Processing
- Communication Systems
- Environmental Sciences & Sustainability

5th Semester

- Wireless Communication
- VLSI and Chip Design
- Transmission Lines & RF Systems
- Professional Elective I
- Professional Elective II
- Mandatory Course I

6th Semester

- Embedded System & IOT Design
- Artificial Intelligence & Machine Learning
- Open Elective I
- Professional Course III
- Professional Course IV
- Mandatory Course II

7th Semester

- Human Values & Ethics
- Elective Management
- Open Elective II
- Open Elective III
- Open Elective IV

8th Semester

- Project Work