Shree Sathyam
College of Engineering and Technology
(An Autonomous Institution)
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai.
Accredited with NAAC (B++) & Recognized under Section 2(f) of UGC
NH-544 Salem – Kochi Highway, Sankari, Salem (DT) - 637301.

Department of Electronics and Communication Engineering

M.E. VLSI DESIGN

Post **Graduate R-2026**

I – Year

Syllabus

SEMESTER - I

P26VDPC11	Graph Theory and Optimization Techniques	L	T	P	S	C
Nature of the Course	Professional Core	3	1	0	3	4
Pre – Requisites	Knowledge of Engineering Mathematics					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts and terminology of graph theory.
2. Develop an understanding of different types of graphs, trees, and graph representations.
3. Study graph traversal techniques and their applications.
4. Understand connectivity, Eulerian and Hamiltonian graphs, and graph colouring.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain the basic concepts, terminology, and representations of graphs.	PO1, PO2	PSO1
CO 2	Analyze	Analyze different types of graphs, subgraphs, paths, circuits, and connectivity.	PO1, PO2	PSO1
CO 3	Apply	Apply graph traversal algorithms such as BFS and DFS to solve computational problems.	PO1, PO2, PO3	PSO1, PSO2
CO 4	Analyze	Analyze trees, spanning trees, minimum spanning trees, and shortest-path problems.	PO1, PO2, PO3	PSO1, PSO2
CO 5	Apply	Apply graph coloring, matching, and related graph-theoretic techniques to engineering problems.	PO1, PO2, PO3, PO4	PSO1, PSO2

Modules

Module - I	**Module Title Advanced Graph Theory**	**L**	**T**	**S**
		9	**0**	**0**
Connectivity & Structure: Menger's Theorem, k-connected graphs, Eulerian and Hamiltonian conditions (Dirac/Ore Theorems). Graph Colorings & Planarity: Brooks' & Vizing's Theorems, Kuratowski's Theorem, chromatic polynomials. Matchings & Covering: Hall's Marriage Theorem, Tutte's 1-Factor Theorem, Konig's Theorem.				
Module – II	**Network Flows & Graph Algorithms**	**L**	**T**	**S**
		9	**0**	**0**
Flow Networks: Max-Flow Min-Cut Theorem, Ford-Fulkerson, Edmonds-Karp, Min-Cost Max-Flow. Shortest Paths & Spanning Trees: Dijkstra's, Floyd-Warshall, Bellman-Ford, Kruskal's, Prim's algorithms. NP-Hard Graph Problems: Traveling Salesperson Problem (TSP), Clique, Vertex Cover formulations.				
Module – III	**Linear & Dual Optimization**	**L**	**T**	**S**
		9	**0**	**0**
Linear Programming Foundations: Standard form, Convex Sets, Basic Feasible Solutions, Simplex & Revised Simplex algorithms. Duality Theory: Dual formulation, Strong Duality, Complementary Slackness, Dual Simplex. Sensitivity Analysis: Perturbations in cost vectors, right-hand side vectors, and constraint matrices.				
Module – IV	**Discrete & Integer Optimization**	**L**	**T**	**S**
		9	**0**	**0**
Integer Linear Programming (ILP): Branch-and-Bound, Branch-and-Cut, Gomory's				

Cutting Plane Algorithm. Classical Discrete Models: Hungarian Algorithm (Assignment), MODI/u-v Method (Transportation), PERT/CPM (Project Scheduling).

Module - V	**Non-Linear & Dynamic Optimization**	**L**	**T**	**S**
		9	**0**	**0**

Unconstrained Optimization: Gradient Descent, Newton-Raphson, Quasi-Newton methods. Constrained Optimization: Convexity, Lagrange Multipliers, Karush-Kuhn-Tucker (KKT) conditions. Dynamic Programming: Bellman's Principle of Optimality, stage-wise formulations (Knapsack, Shortest Path).

Text Books:

1. J. A. Bondy and U. S. R. Murty, Graph Theory, Springer, 2008.
2. Frederick S. Hillier and Gerald J. Lieberman, Introduction to Operations Research, McGraw Hill Education, 12th Edition, 2025.

Reference Books:

1. Douglas B. West, Introduction to Graph Theory, 2nd Edition, Prentice Hall, 2001.
2. Reinhard Diestel, Graph Theory, 5th Edition, Springer, 2017.
3. Hamdy A. Taha, Operations Research: An Introduction, Pearson, 10th Edition, 2017.
4. Bernhard Korte and Jens Vygen, Combinatorial Optimization: Theory and Algorithms, Springer, 5th Edition, 2018.
5. S. S. Rao, Engineering Optimization: Theory and Practice, Wiley, 4th Edition, 2009.

E- Resources:

1. https://nptel.ac.in/courses/111105039
2. https://nptel.ac.in/courses/106105847
3. https://ocw.mit.edu/courses/18-433-combinatorial-optimization-fall-2003/
4. https://ocw.mit.edu/courses/15-053-optimization-methods-in-management-science-spring-2013/

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment			
Bloom's Category	**Internal Assessment Examinations**		**End Semester Examination**
	CIA - I	**CIA- II**	
Remember			
Understand	40		
Apply	20	60	
Analyze	40	40	
Evaluate			
Create			

P26VDPC12	Analog Integrated Circuit Design	L	T	P	S	C
Nature of the Course	Professional core	3	0	0	0	3
Pre – Requisites	Devices and Circuits& Analog Electronics					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts and principles of analog integrated circuit design.
2. Understand the characteristics and operation of MOSFETs and their applications in analog circuits.
3. Analyze and design single-stage and multistage CMOS amplifiers.
4. Study current mirrors, differential amplifiers, and operational amplifiers.
5. Develop the ability to analyze important performance parameters such as gain, bandwidth, noise, power consumption, and stability of analog integrated circuits.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain the basic principles and characteristics of MOS transistors used in analog integrated circuits.	PO1, PO2	PSO1
CO 2	Analyze	Analyze and design CMOS single-stage and multistage amplifiers for specified performance requirements.	PO2, PO3	PSO1, PSO2
CO 3	Analyze	Design and analyze current mirrors, differential amplifiers, and active loads.	PO2, PO3	PSO1, PSO2
CO 4	Analyze	Analyze the architecture and performance of CMOS operational amplifiers and related analog building blocks.	PO2, PO3	PSO1, PSO2
CO 5	Evaluate	Evaluate analog integrated circuits based on gain, bandwidth, noise, power consumption, linearity, and stability.	PO2, PO4, PO5	PSO1, PSO2

Modules

Module - I	**MOS Physics & Single-Stage Amplifiers**	**L**	**T**	**S**
		9	**0**	**0**
MOS Device Modeling: Small-signal models, channel length modulation, body effect, and subthreshold conduction. Basic Amplifiers: Common-Source (CS), Common-Gate (CG), and Source Follower stages with active loads. Cascade Stages: Simple and folded cascade topologies, gain enhancement, and output impedance analysis.				
Module – II	**Current Mirrors, Differential Pairs & Noise**	**L**	**T**	**S**
		9	**0**	**0**
Biasing: Basic, cascade, and Wilson current mirrors; current matching and compliance voltage.Differential Amplifiers: Differential pair with active load, Common-Mode Rejection Ratio (CMRR), and Common-Mode Feedback (CMFB) basics. Noise in Circuits: Thermal and flicker (1/f) noise modeling, input-referred noise calculation for CS and differential stages.				
Module – III	**Operational Amplifiers & Stability**	**L**	**T**	**S**
		9	**0**	**0**
Op-Amp Topologies: Two-stage CMOS Op-Amp, Telescopic, and Folded-Cascade architectures. Performance Metrics: Open-loop gain, unity-gain bandwidth, slew rate, settling time, and PSRR. Frequency Compensation: Stability criteria, phase margin, Miller compensation, pole-splitting, and RHP zero elimination.				

Module – IV	Feedback & Voltage References	L	T	S
		9	0	0

Feedback Topologies: Analysis of four basic feedback configurations and loop gain estimation. Bandgap References: PTAT and CTAT current generation, bandgap reference principle, and supply-independent biasing.

Module - V	Switched-Capacitor Circuits & Layout Principles	L	T	S
		9	0	0

Switched-Capacitor (SC) Fundamentals: MOS switches, charge injection, clock feedthrough, and SC integrators. Analog IC Layout: Device matching techniques (common-centroid, dummy transistors) and substrate noise mitigation.

Text Books:

1. Behzad Razavi, Design of Analog CMOS Integrated Circuits, 2nd Edition, McGraw Hill Education, 2017
2. Paul R. Gray, Paul J. Hurst, Stephen H. Lewis and Robert G. Meyer, Analysis and Design of Analog Integrated Circuits, 6th Edition, John Wiley & Sons, 2024.

Reference Books:

1. Tony Chan Carusone, David A. Johns and Kenneth W. Martin, Analog Integrated Circuit Design, 2nd Edition, John Wiley & Sons, 2012.
2. Phillip E. Allen and Douglas R. Holberg, CMOS Analog Circuit Design, 3rd Edition, Oxford University Press, 2011.
3. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th Edition, Wiley-IEEE Press, 2019.
4. Adel S. Sedra, Kenneth C. Smith and Arun N. Chandorkar, Microelectronic Circuits, 8th Edition, Oxford University Press.
5. Behzad Razavi, Fundamentals of Microelectronics, 2nd Edition, Wiley, 2014.

E- Resources:

1. https://nptel.ac.in/courses/117106030
2. https://nptel.ac.in/courses/117106029
3. https://ocw.mit.edu/courses/6-301-solid-state-circuits-fall-2010/
4. https://ocw.mit.edu/courses/6-331-advanced-circuit-techniques-spring-2002/

TOTAL PERIODS:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment			
Bloom's Category	**Internal Assessment Examinations**		**End Semester Examination**
	CIA - I	**CIA - II**	
Remember			
Understand	40		
Apply			
Analyze	60	60	
Evaluate		40	
Create			

P26VDPC13	Digital CMOS VLSI Design	L	T	P	S	C
Nature of the Course	Professional core	3	0	0	0	3
Pre – Requisites	Digital Electronics &Basics of MOSFET					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts and principles of CMOS VLSI design.
2. Understand CMOS technology, fabrication processes, and design rules.
3. Analyze and design CMOS combinational and sequential digital circuits.
4. Study various CMOS logic styles, memory circuits, and arithmetic circuits.
5. Develop skills to design VLSI circuits considering performance, power consumption, area, and reliability.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain the fundamentals of CMOS technology, fabrication processes, and VLSI design methodologies.	PO1, PO2	PSO1
CO 2	Analyze	Analyze and design CMOS combinational logic circuits using different logic styles.	PO1, PO2, PO3	PSO1, PSO2
CO 3	Apply	Design and analyze sequential circuits such as latches, flip-flops, registers, and counters using CMOS technology.	PO1, PO2, PO3, PO5	PSO1, PSO2
CO 4	Analyze	Analyze and design CMOS arithmetic circuits, memories, and other commonly used VLSI building blocks.	PO1, PO2, PO3, PO5	PSO1, PSO2
CO 5	Evaluate	Evaluate and optimize VLSI circuits based on power, performance, area, and reliability (PPAR) requirements.	PO2, PO3, PO4, PO5	PSO1, PSO2

Modules

Module - I	**MOS Transistors & The CMOS Inverter**	**L**	**T**	**S**
		9	**0**	**0**
MOS Physics & Non-Idealities: Threshold voltage (Vth), body effect, velocity saturation, and short-channel effects (DIBL, subthreshold leakage). CMOS Inverter Analysis: Static transfer characteristics VTC, noise margins, dynamic switching energy, static leakage, and RC delay models. Interconnect Delay: Parasitic resistance/capacitance extraction, Elmore delay estimation, and buffer insertion.				
Module – II	**Combinational Logic Design & Gate Sizing**	**L**	**T**	**S**
		9	**0**	**0**
Logic Design Styles: Static complementary CMOS, pass-transistor logic, and dynamic Domino logic. Logical Effort Method: Delay optimization, path logical/electrical effort, and gate sizing for high capacitive loads. Layout Principles: CMOS design rules (DRC), stick diagrams, and standard cell layouts.				
Module – III	**Sequential Circuits & Clock Timing**	**L**	**T**	**S**
		9	**0**	**0**
Latches & Registers: Multiplexer-based latches, master-slave flip-flops, dynamic C2MOS, and True Single-Phase Clocked (TSPC) circuits. Timing Constraints: Setup time, hold time, clock-to-Q delay, clock skew, and jitter analysis. Clock Distribution: Clock gating and H-tree clock networks.				
Module – IV	**Arithmetic Subsystems & Memory Design**	**L**	**T**	**S**
		9	**0**	**0**
Data Path Units: High-speed adders (Carry-Lookahead, Carry-Select) and Wallace tree multipliers. SRAM Memory Cells: 6T SRAM bit-cell operations, read/write noise margins (SNM), and sense amplifiers				

Module - V	Low-Power Techniques & ASIC/DFT Flow	L	T	S
		9	0	0

Low-Power Design: Dynamic Voltage & Frequency Scaling (DVFS), Multi-Threshold CMOS (MTCMOS), and power gating. Design & Test Flow: ASIC implementation flow (RTL-to-GDSII), Scan-chain insertion, and Design for Testability (DFT) basics.

Text Books:

1. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, 2011.
2. Sung-Mo Kang and Yusuf Leblebici, CMOS Digital Integrated Circuits: Analysis and Design, 3rd Edition, McGraw-Hill Education, 2003.

Reference Books:

1. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th Edition, Wiley-IEEE Press, 2019.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2003.
3. Stephen M. Trimberger, Field-Programmable Gate Array Technology, Springer, 1994.
4. Wayne Wolf, Modern VLSI Design: System-on-Chip Design, 3rd Edition, Pearson Education, 2008.
5. John P. Uyemura, Circuit Design for CMOS VLSI, Springer, 2005.

E- Resources:

1. https://nptel.ac.in/courses/117106092
2. https://nptel.ac.in/courses/117106149
3. https://ocw.mit.edu/courses/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/
4. https://www.coursera.org/learn/vlsi-design
5. https://www.edx.org/learn/vlsi
6. https://www.eecs.umich.edu/courses/eecs427/

Total periods:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment			
Bloom's Category	**Internal Assessment Examinations**		**End Semester Examination**
	CIA - I	**CIA - II**	
Remember			
Understand	40		
Apply	20	20	
Analyze	40	40	
Evaluate		40	
Create			

P26VDPC14	Digital System Design using FPGA	L	T	P	S	C
Nature of the Course	Professional Core	3	0	0	0	3
Pre – Requisites	Digital Logic Design & Fundamentals of Verilog/VHDL					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts of FPGA architecture, technology, and digital system design.
2. Understand FPGA building blocks such as LUTs, flip-flops, logic blocks, routing resources, and I/O blocks.
3. Develop skills in designing combinational and sequential digital circuits using Verilog HDL/VHDL.
4. Understand the FPGA design flow, including RTL design, synthesis, simulation, implementation, and timing analysis.
5. Develop and implement digital systems on FPGA platforms with emphasis on speed, area, power, and reliability.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain FPGA architecture, programmable logic elements, routing resources, and I/O structures.	PO1, PO2	PSO1
CO 2	Apply	Design and model combinational and sequential digital circuits using HDL.	PO1, PO3	PSO1, PSO2
CO 3	Analyze	Develop and simulate RTL designs using Verilog HDL/VHDL and interpret simulation results.	PO2, PO4	PSO1, PSO2
CO 4	Apply	Implement digital systems such as counters, registers, arithmetic units, FSMs, and memory interfaces on FPGA platforms.	PO1, PO3, PO5	PSO1, PSO2
CO 5	Analyze	Analyze and optimize FPGA designs based on timing, area, power, and resource utilization.	PO2, PO3, PO5	PSO1, PSO2

Modules

Module - I	**Advanced Hardware Description Languages (HDL)**	**L**	**T**	**S**
		9	**0**	**0**
Synthesizable RTL: Behavioral, Dataflow, Structural Verilog/System Verilog; synthesizable vs. non-synthesizable constructs. Complex FSM Design: Mealy, Moore, One-Hot state encoding, Sub-FSMs, and FSM with Data Path (FSMD) architectures. Verification: Self-checking testbenches, tasks, functions, and functional simulation strategies.				
Module – II	**FPGA Fabric Architecture**	**L**	**T**	**S**
		9	**0**	**0**
Logic Resources: Look-Up Tables (LUTs), Configurable Logic Blocks (CLBs), Distributed RAM vs. Block RAM (BRAM), DSP slices. Clocking & I/O: Global clock networks, Clock Buffers (BUFG), Phase-Locked Loops (PLLs), Mixed-Mode Clock Managers (MMCMs), and dynamic I/O standards.				
Module – III	**Synthesis & Static Timing Analysis (STA)**	**L**	**T**	**S**
		9	**0**	**0**
Timing Closure: Setup/Hold time math, clock skew, jitter, fmax, and critical path optimization. Constraints (.SDC/.XDC): Primary/generated clocks, input/output delays, false paths, and multi-cycle paths. RTL Optimization: Pipelining, retiming, register balancing, and clock gating.				
Module – IV	**Subsystem & Multi-Clock Design**	**L**	**T**	**S**
		9	**0**	**0**
Memory & Interfaces: Single/Dual-Port Block RAMs, Synchronous and Asynchronous FIFO				

design. Clock Domain Crossing (CDC): Multi-flop synchronizers, handshake protocols, and gray-code counters. System Interconnects: AXI4-Lite/AXI4-Stream protocols and UART/SPI/I2C peripheral controllers.				
Module - V	**Module Title Hardware Debugging & HW/SW Co-Design**	**L**	**T**	**S**
		9	**0**	**0**
Place & Route Flow: Floor planning, pin assignments, placement, routing, bitstream generation, and utilization reports. On-Chip Debugging: Integrated Logic Analyzer (Xilinx ILA / Intel SignalTap) insertion and JTAG boundary-scan testing. Processor Integration: Soft-core processors (RISC-V/Micro Blaze) and Memory-Mapped IP integration.				

Text Books:

1. Stephen Brown and Zvonko Vranesic, Fundamentals of Digital Logic with Verilog Design, 3rd Edition, McGraw-Hill Education, 2014.
2. Michael D. Ciletti, Advanced Digital Design with the Verilog HDL, 2nd Edition, Pearson Education, 2011.

Reference Books:

1. Wayne Wolf, FPGA-Based System Design, Prentice Hall, 2004.
2. Pong P. Chu, FPGA Prototyping by Verilog Examples: Xilinx Spartan-3 Version, Wiley-Interscience, 2008.
3. Clive Maxfield, The Design Warrior's Guide to FPGAs, Elsevier, 2004.
4. Stephen Brown and Zvonko Vranesic, Digital Logic Design: Principles and Practices, 3rd Edition, McGraw-Hill, 2003.
5. Frank Vahid, Digital Design, 2nd Edition, Wiley, 2010.

E- Resources:

1. https://nptel.ac.in/courses/117108040
2. https://nptel.ac.in/courses/108105132
3. https://www.fpga4student.com/
4. https://www.intel.com/content/www/us/en/developer/topic-technology/fpga-academic/materials.html
5. https://docs.amd.com/

Total Periods:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment				
Bloom's Category	**Internal Assessment Examinations**			**End Semester Examination**
	CIA - I	**CIA - II**	**CIA- III**	
Remember				
Understand	40			
Apply	40	40		
Analyze	20	60		
Evaluate				
Create				

P26VDPC15	Semiconductor Device Modelling and Simulation	L	T	P	S	C
Nature of the Course	Professional Core	3	0	0	0	3
Pre – Requisites	Semiconductor Physics , Electronic Device & Basics of Simulation					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts of semiconductor device physics, modelling, and simulation.
2. Understand the electrical characteristics and mathematical models of PN junctions, diodes, BJTs, MOSFETs, and other semiconductor devices.
3. Develop mathematical models for analyzing the behavior of semiconductor devices under different operating conditions.
4. Study numerical techniques used for semiconductor device simulation and analysis.
5. Develop skills to use device simulation tools for analyzing and optimizing semiconductor device performance.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Remember	Explain the fundamental principles of semiconductor physics and device operation.	PO1	PSO1
CO 2	Understand	Develop mathematical and equivalent circuit models for semiconductor devices such as diodes, BJTs, and MOSFETs.	PO1, PO2	PSO1
CO 3	Apply	Apply the electrical characteristics and performance parameters of semiconductor devices using analytical models.	PO1, PO2	PSO1, PSO2
CO 4	Analyze	Analyze numerical methods and simulation techniques to model semiconductor devices under different operating conditions.	PO2, PO4	PSO1, PSO2
CO 5	Evaluate	Use semiconductor device simulation tools to evaluate and optimize device characteristics such as current, voltage, capacitance, power, and switching performance.	PO2, PO3, PO5	PSO1, PSO2

Modules

Module - I	**Semiconductor Physics and Device Fundamentals**	**L**	**T**	**S**
		9	**0**	**0**
Semiconductor materials, energy bands, carrier statistics, carrier concentration, drift and diffusion, mobility, generation and recombination. PN junctions, metal-semiconductor contacts and basic device characteristics.				
Module – II	**Semiconductor Device Equations and Modelling**	**L**	**T**	**S**
		9	**0**	**0**
Poisson equation, continuity equations, drift-diffusion model and boundary conditions. Physical parameters, doping profiles, mobility and recombination models. Basic numerical formulation of semiconductor device models.				
Module – III	**MOS Device Modelling**	**L**	**T**	**S**
		9	**0**	**0**
MOS capacitor, surface potential, threshold voltage and C–V characteristics. MOSFET current-voltage modelling, SPICE models, subthreshold operation and small-signal modelling. Short-channel and narrow-width effects.				

Module – IV	Advanced Device Modelling and Numerical Methods	L	T	S
		9	0	0

Short-channel effects, DIBL, velocity saturation and hot-carrier effects. Numerical solution of device equations, finite-difference methods, mesh generation and Newton-Raphson techniques. Two-dimensional and three-dimensional device modelling.

Module - V	Device Simulation and TCAD	L	T	S
		9	0	0

Introduction to device simulation tools and TCAD methodology. Simulation of PN junction diode, MOS capacitor, MOSFET and BJT. Extraction of electrical characteristics, parameter analysis and simulation of advanced semiconductor devices.

Text Books:

1. S. M. Sze and Kwok K. Ng, Physics of Semiconductor Devices, 3rd Edition, John Wiley & Sons, 2006.
2. D. A. Neamen, Semiconductor Physics and Devices: Basic Principles, 4th Edition, McGraw-Hill Education, 2012.

Reference Books:

1. C. M. Snowden, Introduction to Semiconductor Device Modelling, World Scientific Publishing, 1986.
2. Christopher M. Snowden, Semiconductor Device Modelling, Springer, 1988.
3. S. Selberherr, Analysis and Simulation of Semiconductor Devices, Springer, 1984.
4. Matthew R. Melloch, Michael S. Lundstrom and Francis M. Szmulowicz, Semiconductor Device Fundamentals, Pearson, 2015.
5. J. P. McKelvey, Solid State and Semiconductor Physics, Krieger Publishing, 1984.

E- Resources:

1. https://nptel.ac.in/courses/108105188
2. https://nptel.ac.in/courses/117106033
3. https://ocw.mit.edu/courses/6-012-microelectronic-devices-and-circuits-fall-2005/
4. https://ocw.mit.edu/courses/6-720j-integrated-microelectronic-devices-spring-2007/
5. https://ghzphy.github.io/Sentaurus_Training/sd/sd_menu.html

Total Periods:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment				
Bloom's Category	**Internal Assessment Examinations**			**End Semester Examination**
	CIA - I	**CIA - II**		
Remember	40			
Understand	40			
Apply	20	20		
Analyze		40		
Evaluate		40		
Create				

P26VDPC16	Analog IC Design Laboratory	L	T	P	S	C
Nature of the Course	Professional Core	0	0	4	0	2
Pre – Requisites	MOSFET/BJT fundamentals, circuit simulation using SPICE/EDA tools.					

Course Objectives:

The course is intended to

1. Provide practical knowledge of analog integrated circuit design and analysis.
2. Develop skills in designing and simulating MOSFET-based analog circuits.
3. Analyze the performance of CMOS amplifiers, current mirrors, differential amplifiers, and operational amplifiers.
4. Familiarize students with SPICE-based circuit simulation tools and interpretation of simulation results.
5. Evaluate analog circuits based on gain, bandwidth, power consumption, noise, and stability..

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Apply	Design and simulate basic MOSFET and CMOS analog circuits using circuit simulation tools.	PO1, PO3, PO5	PSO1, PSO2
CO 2	Analyze	Analyze the characteristics and performance of CMOS amplifiers.	PO1, PO2, PO4	PSO1
CO 3	Evaluate	Design and evaluate current mirrors, differential amplifiers, and active loads.	PO1, PO3, PO5	PSO1, PSO2
CO 4	Apply	Design and simulate basic CMOS operational amplifier circuits and determine their performance parameters.	PO1, PO3, PO5	PSO1, PSO2
CO 5	Evaluate	Evaluate and optimize analog IC designs based on gain, bandwidth, power, noise, and stability.	PO1, PO2, PO3, PO5	PSO1, PSO2

List of Experiments

S.No	Exercises	CO Mapping	Bloom's Level
Part A: Front-End Schematic Design & Simulation			
1	**MOS Transistor Characterization:** Extract threshold voltage (Vth), transconductance (gm), output resistance (ro), and channel length modulation (ƛ) from ID vs. VGS and ID vs VDS plots.	CO1	Apply
2	**Single-Stage Amplifiers:** Simulate Common-Source (CS) stages with active current source loads to evaluate DC voltage gain, 3dB bandwidth, and output swing.	CO2	Analyze
3	**High-Impedance Cascode Amplifiers:** Design simple and folded-cascode amplifier stages for maximum output impedance and gain enhancement	CO2	Analyze
4	**Current Mirrors & Biasing Networks:** Evaluate basic, cascode, and Wilson current mirrors for current matching accuracy, minimum compliance voltage, and output resistance	CO3	Evaluate
5	**CMOS Differential Pair:** Measure Differential Gain, Common-Mode Gain, Common-Mode Rejection Ratio (CMRR), and Input Common-Mode Range (ICMR).	CO2	Analyze
6	**Two-Stage CMOS Operational Amplifier:** Design a two-stage Op-Amp targeting specified parameters (Av > 60 dB, Slew Rate, GBW, and Power Dissipation).	CO2	Analyze

7	**Frequency Compensation & Stability:** Implement Miller compensation and a nulling resistor to eliminate the Right-Half-Plane (RHP) zero and achieve >600 Phase Margin	CO4	Apply
8	**Bandgap Reference (BGR):** Simulate PTAT/CTAT current generators and produce a temperature-independent reference voltage (≈ 1.2V).	CO3	Evaluate
9	**Switched-Capacitor Integrator:** Analyze MOS sampling switch non-idealities (charge injection, clock feedthrough) and design a parasitic-insensitive switched-capacitor integrator	CO4	Apply
Part B: Back-End Physical Layout & Verification			
10	**Analog Custom Layout Design:** Draw physical mask layouts for a CMOS differential pair and current mirror using common-centroid, interdigitation, and guard ring placement.	CO5	Evaluate
11	**Physical Verification (DRC & LVS):** Perform Design Rule Checking (DRC) and Layout Versus Schematic (LVS) comparison to ensure layout-schematic structural equivalence.	CO5	Evaluate
12	**Parasitic Extraction (PEX) & Post-Layout Simulation:** Extract parasitic R and C elements and execute back-annotated simulations to verify gain, bandwidth, and phase margin degradation against pre-layout schematics.	CO5	Evaluate

List of Equipment for a Batch of 30 Students

S.No	Description	Particulars
1.	Computers / Workstations	15 Nos.
2.	Analog Circuit Simulation Software	Cadence Virtuoso / LTspice/Ngspice- 15 Licenses/Installations
3.	Digital Storage Oscilloscopes	15 Nos.
4.	Dual Channel DC Power Supply	15 Nos.
5.	Digital Multimeters	15 Nos.

Total: 60 Periods

E- Resources:

1. https://nptel.ac.in/courses/117106030
2. https://ocw.mit.edu/courses/6-301-solid-state-circuits-fall-2010/
3. https://ocw.mit.edu/courses/6-331-advanced-circuit-techniques-spring-2002/

Assessment

Summative Assessment based on Continuous and End Semester Examination		
Bloom's Level	**Rubric based Continuous Assessment [50 marks]**	**End Semester Examination [50 marks]**
Remember		
Understand		
Apply	12	12
Analyze	16	16
Evaluate	22	22
Create		

P26VDPC17	Digital System Design using FPGA Laboratory	L	T	P	S	C
Nature of the Course	Professional Core	0	0	4	0	2
Pre – Requisites	Digital System Design, Verilog/VHDL programming					

Course Objectives:

The course is intended to

1. Provide practical knowledge of FPGA-based digital system design.
2. Develop skills in designing and coding digital circuits using Verilog HDL/VHDL.
3. Familiarize students with RTL design, simulation, synthesis, and FPGA implementation.
4. Implement combinational and sequential digital systems on an FPGA development board.
5. Analyze FPGA designs based on timing, area, power, and resource utilization.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Apply	Develop and simulate digital circuits using Verilog HDL/VHDL.	PO1, PO2, PO5	PSO1
CO 2	Apply	Design and implement combinational and sequential circuits on an FPGA platform.	PO1, PO3, PO5	PSO1, PSO2
CO 3	Apply	Develop and implement counters, registers, arithmetic circuits, and finite state machines (FSMs) using FPGA.	PO1, PO3, PO5	PSO1, PSO2
CO 4	Analyze	Perform synthesis, implementation, timing analysis, and hardware verification of FPGA designs.	PO2, PO4, PO5	PSO1, PSO2
CO 5	Evaluate	Evaluate and optimize FPGA-based designs considering speed, area, power, and resource utilization.	PO2, PO3, PO4, PO5	PSO1, PSO2

List of Experiments

S.No	Exercises	CO Mapping	Bloom's Level
Part A: Advanced RTL Modeling & System Verilog Verification			
1	**Parameterized Arithmetic Logic Unit (ALU)** • Design a parameterizable ALU (8/16/32-bit) supporting signed/unsigned arithmetic and bitwise operations. • Write a self-checking SystemVerilog testbench utilizing tasks, functions, and dynamic arrays.	CO1	Apply
2	**Finite State Machine with Data Path (FSMD):** • Model a complex controller (e.g., Traffic Light Controller, Vending Machine, or DRAM Controller) using One-Hot Encoding. • Verify state machine behavior, hazard-free transitions, and testbench edge cases.	CO1	Apply
3	**Pipelined Multiplier Engine:** • Design a 4-stage pipelined 16 times 16 array tree multiplier. • Verify throughput improvements against a non-pipelined architectural equivalent.	CO2	Apply
Part B: Multi-Clock Domain & Memory Architectures			
4	**Asynchronous FIFO (Clock Domain Crossing):** • Implement a dual-clock Asynchronous FIFO using dual-port RAM. • Integrate Gray-code read/write counters and two-flop synchronizers to prevent metastability**.**	CO3	Apply

5	**On-Chip Block Memory (BRAM & Distributed RAM):** • Model single-port and true dual-port RAM units. • Compare physical resource synthesis utilization (LUTs, FF vs. Block RAM IP primitives**).**	CO3	Apply
Part C: Constraints, Timing Closure & STA			
6	**Static Timing Analysis (STA) & Constraints (.XDC/.SDC):** • Write timing constraints for primary clocks, input/output delays, false paths, and multi-cycle paths. • Generate post-synthesis Setup/Hold timing reports and resolve timing violations via register balancing and retiming.	CO4	Analyze
7	**Phase-Locked Loop (PLL) & Multi-Clock Generation:** • Instantiate on-chip MMCM / PLL IP cores to generate multiple derived clock frequencies from a board source oscillator	CO4	Analyze
Part D: Hardware Interfaces & On-Chip Debugging			
8	**Communication Controllers:** • Design custom RTL hardware modules for UART (Baud Rate Generator, Transmitter, Receiver), SPI, or I2C protocols. • Establish real-time communication between the FPGA target board and external peripherals	CO5	Evaluate
9	**Integrated Logic Analyzer (ILA) Real-Time Debugging:** • Insert vendor debugging cores (Xilinx ILA / Intel Signal Tap) into a running RTL design. • Set dynamic trigger conditions to capture live internal hardware signals over a JTAG interface.	CO5	Evaluate
Part E: System-Level & Hardware/Software Co-Design			
10	**Soft-Core Processor & AXI Interconnect Integration:** • Instantiate a 32-bit RISC-V or Micro Blaze soft processor core on the FPGA target. • Interface custom hardware peripherals via an AXI4-Lite bus interface and write embedded C code to control hardware IP registers.	CO5	Evaluate
11	**DSP Application Accelerator:** • Design a 4-tap FIR filter or 2D Image Convolution engine mapped onto on-chip DSP48 slices. • Validate real-time processing performance on target FPGA hardware.	CO5	Evaluate

List of Equipment for a Batch of 30 Students

S.No	Description	Particulars
1.	FPGA Development Boards	Xilinx Artix-7 / Zynq-7000 or Intel FPGA – 15 Nos.
2.	Computers / Workstations	Intel Core i5/i7, 8 GB RAM or above – 15 Nos.
3.	Digital Storage Oscilloscopes	15 Nos.
4.	Digital Multimeters	15 Nos.
5.	FPGA Design & Verification Software	Xilinx Vivado / Intel Quartus Prime, ModelSim/Questa – 15 Licenses/Installations

Total: 60 Periods

E- Resources:

1. https://www.amd.com/en/products/software/adaptive-socs-and-fpgas/vivado.html
2. https://www.intel.com/content/www/us/en/software/programmable/quartus-prime/overview.html
3. https://standards.ieee.org/ieee/1800/10860/

Assessment

Summative Assessment based on Continuous and End Semester Examination		
Bloom's Level	**Rubric based Continuous Assessment [50 marks]**	**End Semester Examination [50 marks]**
Remember		
Understand		
Apply	23	23
Analyze	09	09
Evaluate	18	18
Create		

SEMESTER - II

P26VDPC21	Low Power VLSI Design	L	T	P	S	C
Nature of the Course	Professional Core	3	0	0	0	3
Pre – Requisites	Digital Electronics & CMOS/VLSI Design					

Course Objectives:

The course is intended to

1. Introduce the fundamental concepts and challenges of low-power VLSI circuit design.
2. Understand different sources of power dissipation in CMOS circuits.
3. Analyze and apply various power reduction techniques at circuit, logic, architectural, and system levels.
4. Study low-power design techniques for combinational and sequential CMOS circuits.
5. Develop the ability to design energy-efficient VLSI systems while maintaining required performance, area, and reliability

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain the sources of power dissipation in CMOS VLSI circuits and identify major low-power design challenges.	PO1, PO2	PSO1
CO 2	Analyze	Analyze the relationship between power, performance, and area (PPA) in VLSI circuits.	PO1, PO2, PO4	PSO1, PSO2
CO 3	Apply	Apply circuit-level techniques such as voltage scaling, transistor sizing, clock gating, and power gating to reduce power consumption.	PO1, PO2, PO3	PSO1, PSO2
CO 4	Evaluate	Analyze and design low-power combinational and sequential CMOS circuits.	PO1, PO3, PO4	PSO1, PSO2
CO 5	Evaluate	Evaluate and optimize VLSI designs using appropriate low-power techniques while satisfying performance and area constraints.	PO2, PO3, PO4, PO5	PSO1, PSO2

Modules

Module - I	**Fundamentals of Low-Power VLSI**	**L**	**T**	**S**
		9	**0**	**0**
Introduction to low-power VLSI design, sources of power dissipation in CMOS circuits, dynamic and static power consumption, leakage mechanisms, short-circuit power, power-delay product, technology scaling, and the impact of process variations on power consumption.				
Module – II	**Circuit-Level Low-Power Design Techniques**	**L**	**T**	**S**
		9	**0**	**0**
Supply voltage scaling, threshold voltage optimization, transistor sizing, Multi-Threshold CMOS (MTCMOS), Variable Threshold CMOS (VTCMOS), leakage reduction techniques, adiabatic logic, energy recovery circuits, and low-power CMOS design methodologies.				
Module – III	**Logic and Architectural Power Optimization**	**L**	**T**	**S**
		9	**0**	**0**
Clock gating, power gating, operand isolation, bus encoding techniques, low-power combinational and sequential circuit design, memory power optimization, low-power arithmetic units, and architectural techniques for reducing switching activity.				

Module – IV	System-Level Low-Power Design	L	T	S
		9	0	0

Dynamic Voltage and Frequency Scaling (DVFS), multi-voltage and multi-frequency systems, power-aware embedded system design, battery-aware optimization, thermal management, energy-efficient System-on-Chip (SoC) design, and power management strategies.

Module - V	Low-Power Design Methodologies and CAD Tools	L	T	S
		9	0	0

Low-power design flow, power estimation and analysis techniques, Unified Power Format (UPF), Common Power Format (CPF), low-power verification, optimization using Electronic Design Automation (EDA) tools, and case studies of modern low-power VLSI systems.

Text Books:

1. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolić, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Pearson Education, 2003.
2. Kaushik Roy and Sharat Prasad, Low-Power CMOS VLSI Circuit Design, Wiley-Interscience, 2000.

Reference Books:

1. Anantha P. Chandrakasan and Robert W. Brodersen, Low Power Digital CMOS Design, Springer, 1995.
2. Gary K. Yeap, Practical Low Power Digital VLSI Design, Kluwer Academic Publishers, 1998.
3. J. Rabaey, Low Power Design Essentials, Springer, 2009.
4. Dimitrios Soudris, Chirstian Piguet and Costas Goutis, Designing CMOS Circuits for Low Power, Springer, 2002.
5. Neil H. E. Weste and David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, 4th Edition, Pearson Education, 2011.

E- Resources:

1. https://nptel.ac.in/courses/106105034
2. https://nptel.ac.in/courses/117101004
3. https://archive.nptel.ac.in/courses/106/105/106105034/

Total Periods:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment				
Bloom's Category	**Internal Assessment Examinations**			**End Semester Examination**
	CIA - I	**CIA - II**	**CIA- III**	
Remember				
Understand	40			
Apply	20	20		
Analyze	40			
Evaluate		80		
Create				

P26VDPC22	Design for Verification using UVM	L	T	P	S	C
Nature of the Course	Professional Core	3	0	0	0	3
Pre – Requisites	Digital Logic Design, VLSI Design, Verilog/System Verilog HDL					

Course Objectives:

The course is intended to

1. To provide the students complete understanding on UVM testing
2. To become proficient at UVM verification,
3. To provide an experience on self- checking UVM test benches

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Understand the basic concepts of two methodologies UVM	PO1, PO2	PSO1
CO 2	Apply	Build actual verification components.	PO1, PO3, PO5	PSO1, PSO2
CO 3	Apply	Generate the register layer classes.	PO1, PO3, PO5	PSO1, PSO2
CO 4	Analyze	Code test benches using UVM.	PO1, PO2, PO3, PO5	PSO1, PSO2
CO 5	Analyze	Understand advanced peripheral bus testbenches.	PO1, PO2, PO3, PO5	PSO1, PSO2

Modules

Module - I	**Fundamentals of Design Verification**	**L**	**T**	**S**
		9	**0**	**0**
Introduction to VLSI verification, verification challenges, verification planning, verification methodologies, simulation-based verification, directed and constrained-random testing, System Verilog language fundamentals, object-oriented programming concepts, and functional verification flow.				
Module – II	**UVM Architecture and Testbench Development**	**L**	**T**	**S**
		9	**0**	**0**
Overview of Universal Verification Methodology (UVM), UVM components, factory mechanism, configuration database, transaction-level modeling (TLM), sequences and sequencers, drivers, monitors, agents, environments, scoreboards, and reusable verification components.				
Module – III	**Functional Verification and Coverage**	**L**	**T**	**S**
		9	**0**	**0**
Constrained-random stimulus generation, assertions, functional coverage, code coverage, coverage-driven verification, register abstraction layer (RAL), verification IP (VIP), debugging techniques, and verification closure methodologies.				
Module – IV	**Advanced UVM Techniques**	**L**	**T**	**S**
		9	**0**	**0**
Advanced sequence control, virtual sequences, callbacks, objection mechanism, synchronization, phase management, reporting and logging, reusable verification environments, SoC verification concepts, and low-power verification fundamentals.				
Module - V	**Verification Automation and Industry Applications**	**L**	**T**	**S**
		9	**0**	**0**
Verification planning and management, regression testing, scripting and automation, integration with EDA verification tools, hardware acceleration and emulation basics, continuous integration for verification, verification metrics, and case studies on industrial ASIC and FPGA verification using UVM.				

Text Books:

1. Sasan Iman, System Verilog for Verification: A Guide to Learning the Testbench Language Features, 3rd Edition, Springer, 2013.
2. Chris Spear and Greg Tumbush, System Verilog for Verification: A Guide to Learning the Testbench Language Features, 4th Edition, Springer, 2017.

Reference Books:

1. Book title, Author of the Book, Publisher, Version (if Any), Year of Publication
2. Reference Book 02
3. Reference Book 03 Ray Salemi, the UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, 2nd Edition, 2013.
4. Clifford E. Cummings, System Verilog Assertions and Functional Coverage, Sunburst Design.
5. Janick Bergeron, Writing Testbenches: Functional Verification of HDL Models, Springer, 2003.
6. Sutherland, Davidmann and Flake, System Verilog 3.1a: Language Reference Manual, Accellera, 2004.
7. IEEE, IEEE Standard for System Verilog—Unified Hardware Design, Specification, and Verification Language (IEEE 1800), IEEE, 2017.

E- Resources:

1. https://www.accellera.org/community/uvm
2. https://www.accellera.org/activities/working-groups/uvm
3. https://accellera.org/images/downloads/standards/uvm/uvm_users_guide_1.1.pdf
4. https://www.accellera.org/resources/videos/uvm-tutorial-2014
5. https://github.com/accellera-official/uvm-core
6. https://www.uvmkit.com/

Total Periods:45

Assessment

Formative assessment			
Bloom's Level	**Assessment Component**	**Marks**	**Total marks**
Knowledge Demonstration			
Remember	Quiz	5	10
Understand	Tutorial Class / Assignment		
	Attendance	5	

Summative Assessment				
Bloom's Category	**Internal Assessment Examinations**			**End Semester Examination**
	CIA - I	**CIA - II**		
Remember				
Understand	40			
Apply	60	20		
Analyze		80		
Evaluate				
Create				

P26VDPC23	System-on-Chip (SoC) Design	L	T	P	S	C
Nature of the Course	Professional Core	3	0	2	0	4
Pre – Requisites	Digital Electronics, HDL Programming (Verilog/VHDL)					

Course Objectives:

The course is intended to

1. Understand the architecture and design principles of System-on-Chip (SoC).
2. Study SoC components, buses, memories, processors and peripherals.
3. Learn RTL design and IP-based SoC integration.
4. Understand verification, testing and power-aware SoC design.
5. Gain knowledge of FPGA/ASIC-based SoC implementation.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Understand	Explain the architecture and design flow of System-on-Chip.	PO1, PO2	PSO1
CO 2	Analyze	Analyze processors, memories and on-chip interconnects used in SoC.	PO1, PO2, PO3	PSO1, PSO2
CO 3	Apply	Design and integrate IP cores and peripherals in an SoC.	PO1, PO3, PO5	PSO1, PSO2
CO 4	Apply	Apply verification and testing techniques for SoC designs.	PO2, PO4, PO5	PSO1, PSO2
CO 5	Analyze	Analyze low-power techniques and implement SoC designs using FPGA/ASIC platforms.	PO1, PO2, PO3, PO5	PSO1, PSO2

Modules

Module - I	**INTRODUCTION TO SYSTEM-ON-CHIP**	**L**	**T**	**S**
		9	**0**	**0**
SoC concepts and evolution, SoC architecture, design challenges, hardware and software partitioning, SoC design flow, IP cores, reusable IP, processor cores, memories, peripherals and interfaces. SoC design methodologies and applications.				
Module – II	**PROCESSOR, MEMORY AND INTERCONNECT ARCHITECTURE**	**L**	**T**	**S**
		9	**0**	**0**
Embedded processors and processor cores, RISC and CISC concepts, multicore SoC, memory hierarchy, cache and memory controllers, on-chip communication, bus architectures, AMBA protocols, AXI, AHB and APB, Network-on-Chip fundamentals.				
Module – III	**SoC DESIGN AND INTEGRATION**	**L**	**T**	**S**
		9	**0**	**0**
RTL-based SoC design, IP integration, hardware/software co-design, clock and reset management, DMA controllers, timers, UART, SPI, I²C and GPIO interfaces. Address mapping, register design, interrupt controllers and peripheral integration.				
Module – IV	**SOC VERIFICATION AND TESTING**	**L**	**T**	**S**
		9	**0**	**0**
SoC verification methodologies, simulation and functional verification, constrained-random verification, assertion-based verification, UVM fundamentals, verification of IP and interfaces, coverage analysis, design-for-testability, scan testing, BIST and SoC debugging.				
Module – V	**LOW-POWER SOC AND IMPLEMENTATION**	**L**	**T**	**S**
		9	**0**	**0**
Low-power SoC design techniques, clock gating, power gating, voltage scaling, multi-voltage design, power management, physical design considerations, timing and signal integrity, FPGA-based SoC implementation, ASIC implementation, reliability and security issues in SoC.				

Laboratory Components

S.No	List of Exercises	CO Mapping	RBT
1	**SoC Architecture Design:** Design a basic SoC with a processor, memory, interconnect, and peripherals.	CO1, CO2	Analyze
2	**IP Core Integration:** Design a custom IP core and integrate it with the SoC using AXI, AHB, or APB protocols.	CO2, CO3	Apply
3	**Hardware/Software Co-Design:** Integrate a hardware accelerator with the SoC and develop simple software to control it.	CO3	Create
4	**SoC Verification:** Verify an SoC module using SystemVerilog/UVM, assertions, and functional coverage.	CO4	Evaluate
5	**Low-Power SoC Implementation:** Apply clock gating and power optimization techniques and implement the design on an FPGA/ASIC platform.	CO5	Evaluate

Total: 30 Periods

Text Books:

1. Ross K. Snider, Advanced Digital System Design using SoC FPGAs: An Integrated Hardware/Software Approach, Springer, 2023. This book specifically covers advanced digital system design using SoC FPGAs and hardware/software integration.
2. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, 2nd Edition, Prentice Hall, 2003.
3. Rene Beuchat, Florian Depraz, Sahand Kashani and Andrea Guerrieri, Fundamentals of System-on-Chip Design on Arm Cortex-M Microcontrollers, Arm Education Media. It covers processor architectures, AMBA, interconnects, peripherals and memory

Reference Books:

1. Prakash Rashinkar, Peter Paterson and Leena Singh, System-on-a-Chip Verification: Methodology and Techniques, Kluwer Academic Publishers, 2001.
2. Grant Martin and Henry Chang, Winning with IP: Managing Intellectual Property Today, Springer, 2002.
3. Chris Spear and Greg Tumbush, SystemVerilog for Verification: A Guide to Learning the Testbench Language Features, 3rd Edition, Springer, 2015.
4. Ray Salemi, The UVM Primer: A Step-by-Step Introduction to the Universal Verification Methodology, Accellera, 2013.
5. R. Jacob Baker, CMOS: Circuit Design, Layout, and Simulation, 4th Edition, Wiley-IEEE Press, 2019.
6. Jan M. Rabaey, Anantha Chandrakasan and Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Prentice Hall, 2nd Edition, 2003.

E- Resources:

1. https://ocw.mit.edu/courses/6-884-complex-digital-systems-spring-2005/
2. https://ocw.mit.edu/courses/6-823-computer-system-architecture-fall-2005/
3. https://ocw.mit.edu/courses/6-374-analysis-and-design-of-digital-integrated-circuits-fall-2003/
4. https://www.nptel.ac.in/courses/108102045
5. https://www.accellera.org/downloads/standards

Assessment

Summative assessment					
Bloom's Level	**Continuous Assessment**				**End Semester Examination (Theory)**
	Theory Marks			**Practical**	
	CIA - I	**CIA - II**	**Attendance**	**Rubric based CIA**	
Remember					
Understand	20				10
Apply	10	30		10	40
Analyse	20	20		10	20
Evaluate				20	10
Create				10	10

P26VDPC24	Verification using UVM Laboratory	L	T	P	S	C
Nature of the Course	Professional Core	0	0	4	0	2
Pre – Requisites	Verilog HDL, RTL Design and Simulation					

Course Objectives:

The course is intended to

1. Develop proficiency in System Verilog constructs required for modern hardware verification and testbench development.
2. Understand and apply the Universal Verification Methodology (UVM) for developing reusable and scalable verification environments.
3. Design and implement UVM verification components such as sequences, sequencers, drivers, monitors, agents, scoreboards, and environments.
4. Apply constrained-random verification, assertions, and functional coverage to verify the functionality and performance of digital designs.
5. Develop complete UVM-based verification environments for industry-standard digital interfaces and analyze verification results.

Course Outcomes:

On successful completion of the course, students will be able to

S.No	Bloom's Level	Course Outcome	PO	PSO
CO 1	Apply	Develop and simulate System Verilog test benches for digital designs.	PO1, PO2, PO5	PSO1
CO 2	Apply	Build UVM verification components such as drivers, monitors, agents, and scoreboards.	PO1, PO3, PO5	PSO1, PSO2
CO 3	Apply	Apply constrained-random and assertion-based verification techniques.	PO1, PO2, PO4, PO5	PSO1, PSO2
CO 4	Apply	Develop UVM Register Layer (RAL) models for register verification.	PO1, PO3, PO5	PSO1, PSO2
CO 5	Evaluate	Design and verify digital IP cores and interfaces using complete UVM verification environments.	PO2, PO3, PO4, PO5	PSO1, PSO2

List of Experiments

S.No	Exercises	CO Mapping	Bloom's Level
1	Write a System Verilog interface and test bench with constrained random stimulus generation for a simple DUT.	CO1, CO3	Apply
2	Develop functional coverage (cover groups and coverpoints) and System Verilog Assertions (SVA) for a DUT.	CO1, CO3	Apply
3	Design a UVM sequence item and sequence, and execute it through a UVM sequencer.	CO2	Apply
4	Develop a UVM driver and monitor, and integrate them with a sequencer to form a UVM agent.	CO2	Apply
5	Build a UVM environment connecting the agent to a scoreboard using TLM analysis ports	CO2	Apply
6	Configure a UVM test bench using UVM-config_db for virtual interface and parameter passing.	CO2	Apply
7	Design a complete UVM testbench (agent, scoreboard, coverage) for a synchronous FIFO.	CO2, CO5	Apply
8	Implement UVM factory overrides for component and sequence substitution.	CO2	Apply

9	Design a virtual sequence and virtual sequencer for multi-interface coordination.	CO 4	Apply
10	Develop a UVM-based verification environment (with RAL) for a simple protocol such as APB or SPI.	CO4, CO5	Apply

List of Equipment for a Batch of 30 Students

S.No	Description	Particulars
1.	Computers / Workstations	Intel Core i5/i7, 8 GB RAM or above – 15 Nos.
2.	System Verilog / UVM Simulation Software	QuestaSim / ModelSim / VCS – 15 Licenses/Installations
3.	FPGA Development Boards	Xilinx Artix-7 / Zynq-7000 or equivalent – 15 Nos
4.	Logic Analyzer / Digital Oscilloscope	100 MHz or above – 15 Nos.
5.	Digital Multimeters	Standard laboratory type – 15 Nos.

Total: 60 Periods

E- Resources:

1. https://www.accellera.org/community/uvm
2. https://www.accellera.org/activities/working-groups/uvm
3. https://standards.ieee.org/ieee/1800/7743/
4. https://verificationacademy.com/
5. https://github.com/accellera-official/uvm-core

Assessment

Summative Assessment based on Continuous and End Semester Examination		
Bloom's Level	**Rubric based Continuous Assessment [50 marks]**	**End Semester Examination [50 marks]**
Remember		
Understand		
Apply	50	50
Analyze		
Evaluate		
Create		