Shree Sathyam
College of Engineering and Technology
(An Autonomous Institution)

Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai.
Accredited with NAAC (B++) & Recognized under Section 2(f) of UGC
NH-544 Salem – Kochi Highway, Sankari, Salem (DT) - 637301.

Regulation : SSCET R- 2026

Programme: M.E.,VLSI-Design

Vision

To be recognized by society as a full-fledged department offering a quality higher education in the Communication Engineering field with a research focus to stay in tune with advancing technology.

Mission

- To engage modern education aids, laboratories, and competent faculty to ensure effective teaching and learning processes to meet the ever-growing and changing industrial and business environment challenges.
- To provide industry-institute interactions to strengthen the technical skills of the students and prepare them for the workforce and as entrepreneurs.
- To enable graduates to develop into the ethical, skilled hardware and software engineers that industry need, with a focus on values that improve society.

Abbreviations

BS- Basic Science Courses

CAT-Category ;**CT**-Course Type

CIA- Continuous Internal Assessment

EE-Competency Enhancement Courses

ESE- End Semester Examination

ET-Emerging Technology Elective Courses

HS-Humanities and Social Sciences

IOC-Industry Oriented Courses

L – Laboratory Course

LIT – Laboratory Integrated Theory

MC-Mandatory Non-Credit Courses

OE-Open Elective Courses

PC-Professional Core Courses

PE-Professional Elective Courses

S-Self study

SD – Skill Development

T – Theory

TCP – Total Contact Period

PROGRAM EDUCATIONAL OBJECTIVES (PEOs)	
PEO1	Apply advanced VLSI knowledge to solve complex design problems and develop innovative solutions.
PEO2	Design, analyze, verify, and implement reliable VLSI systems using modern EDA tools and emerging technologies.
PEO3	Pursue research, innovation, lifelong learning, ethical practices, teamwork, and leadership to meet industrial and societal needs.

PROGRAM OUTCOMES(POs)	
PO1	**Engineering Knowledge**: Apply math, science, and engineering fundamentals to complex problems.
PO2	**Problem Analysis**: Identify and analyze complex problems using research and sustainability principles.
PO3	**Design Solutions**: Design systems and processes considering health, safety, cost, culture, and environment.
PO4	**Investigations**: Use experiments, modelling, and data analysis to reach valid conclusions.
PO5	**Engineering Tools**: Apply modern tools for modelling and problem-solving, recognizing their limits.
PO6	**Society & Environment**: Assess societal, legal, and environmental impacts of engineering solutions.
PO7	**Ethics**: Commit to ethics, human values, diversity, and legal compliance.
PO8	**Teamwork**: Work effectively as an individual and in multidisciplinary teams.
PO9	**Communication**: Communicate clearly in reports, presentations, and documentation across diverse groups.
PO10	**Management & Finance**: Apply management and economic principles in projects and teamwork.
PO11	**Lifelong Learning**: Engage in continuous learning, adapt to new technologies, and think critically.

PROGRAM SPECIFIC OUTCOME (PSOs)	
PS01	Apply advanced VLSI knowledge to design and develop innovative semiconductor and VLSI systems.
PSO2	Analyze, verify, and implement reliable VLSI designs using modern EDA tools and emerging technologies.

Semester - I													
S. No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
	THEORY												
1.	P26VDPC11	Graph Theory and Optimization Techniques	BS	T	3	1	0	3	4	4	40	60	100
2.	P26VDPC12	Analog IC Design	PC	T	3	0	0	-	3	3	40	60	100
3.	P26VDPC13	Digital CMOS VLSI Design	PC	T	3	0	0	-	3	3	40	60	100
4.	P26VDPC14	Digital System Design using FPGA	PC	T	3	0	0	-	3	3	40	60	100
5.	P26VDPC15	Semiconductor Devices and Modelling	PC	T	3	0	0	-	3	3	40	60	100
6.		Mandatory Course-I*	MC	T	3	0	0	-	0	3	100	-	100
	LABORATORY												
7.	P26VDPC16	Analog IC Design Laboratory	PC	L	0	0	4	-	2	4	60	40	100
8.	P26VDPC17	Digital System Design using FPGA Laboratory	PC	L	0	0	4	-	2	4	60	40	100
	COMPETENCY ENHANCEMENT												
9.	P26VDEE11	Technical Seminar	EE	L	0	0	2	-	1	2	100	-	100
								Total	**21**	**29**	**520**	**380**	**900**

*Mandatory Course-I is a Non-credit Course (Student shall select one course from the list given under Mandatory Course-I)

Semester - II													
S. No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
	THEORY												
1.	P26VDPC21	Low Power VLSI Design	PC	T	3	0	0	-	3	3	40	60	100
2.	P26VDPC22	Design for Verification using UVM	PC	T	3	0	0	-	3	3	40	60	100
3.		Professional Elective -I	PE	T	3	0	0	-	3	3	40	60	100
4.		Professional Elective -II	PE	T	3	0	0	-	3	3	40	60	100
5.		Mandatory Course-II	MC	T	3	0	0	-	0	3	100	-	100
	LABORATORY INTEGRATED THEORY												
6.	P26VDPC23	System-on-Chip (SoC) Design	PC	LIT	3	0	2	-	4	5	50	50	100
	LABORATORY												
7.	P26VDPC24	Verification using UVM Laboratory	PC	L	0	0	4	-	2	4	60	40	100
	SKILL DEVELOPMENT COURSE												
8.	P26VDSD21	Industry Oriented Course	SD	LIT	1	0	2	-	2	3	100	-	100
9.	P26VDSD22	Mini Project	SD	L	0	0	2	-	2	2	100	-	100
								Total	**22**	**29**	**570**	**330**	**900**

*Mandatory Course-II is a Non-credit Course (Student shall select one course from the list given under Mandatory Course-II)

Semester - III													
S. No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
	THEORY												
1.	P26VDPC31	Research Methodology & IPR	PC	T	3	0	0	-	3	3	40	60	100
2.		Professional Elective- III	PC	T	3	0	0	-	3	3	40	60	100
3.		Professional Elective –IV	PE	T	3	0	0	-	3	3	40	60	100
4.		Emerging Technology-Elective	ET	T	3	0	0	-	3	3	40	60	100
	SKILL DEVELOPMENT COURSE												
5.	P26VDSD31	Project Work - Phase I	SD	L	0	0	12	-	6	12	100	-	100
	COMPETENCY ENHANCEMENT												
6.	P26VDEE31	Research Paper Review and Presentation	EE	L	0	0	2	-	1	2	100	-	100
								Total	**19**	**26**	**360**	**240**	**600**

Semester - IV													
S.No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1.	P26VDSD41	Project Work - Phase II	SD	L	0	0	24	0	12	24	60	40	100
				Total	**0**	**0**	**24**	**0**	**12**	**24**	**60**	**40**	**100**

TOTAL CREDITS TO BE EARNED FOR THE AWARD OF THE DEGREE = 74

CREDIT SUMMARY

S.No	Category	Semester wise Credit Allocation					
		I	II	III	IV	Total Credits (SSCET)	Credits in %
1.	BS	4				4	5.40
2.	MC	0	0			0	0.0
3.	PC	16	12	03		31	41.89
4.	EE	01		01		2	2.70
5.	PE		06	06		12	16.22
6.	ET			03		3	4.05
7.	SD		04	06	12	22	29.73
Total		**21**	**22**	**19**	**12**	**74**	**100.0**

Professional Core Course(PC)													
S. No	**Course Code**	**Course Name**	**CAT**	**CT**	**Period / Week**						**Maximum Marks**		
					L	**T**	**P**	**S**	**C**	**TCP**	**CIA**	**ESE**	**Total**
1	P26VDPC12	Analog IC Design	PC	T	3	0	0	-	3	3	40	60	100
2	P26VDPC13	Digital CMOS VLSI Design	PC	T	3	0	0	-	3	3	40	60	100
3	P26VDPC14	Digital System Design using FPGA	PC	T	3	0	0	-	3	3	40	60	100
4	P26VDPC15	Semiconductor Devices and Modelling	PC	T	3	0	0	-	3	3	40	60	100
5	P26VDPC16	Analog IC Design Laboratory	PC	L	0	0	4	-	2	4	60	40	100
6	P26VDPC17	Digital System Design using FPGA Laboratory	PC	L	0	0	4	-	2	4	60	40	100
7	P26VDPC21	Low Power VLSI Design	PC	T	3	0	0	-	3	3	40	60	100
8	P26VDPC22	Design for Verification using UVM	PC	T	3	0	0	-	3	3	40	60	100
9	P26VDPC23	System-on-Chip (SoC) Design	PC	LIT	2	0	2	-	4	4	50	50	100
10	P26VDPC24	Verification using UVM Laboratory	PC	L	0	0	4	-	2	4	60	40	100
11	P26VDPC31	Research Methodology & IPR	PC	T	3	0	0	-	3	3	40	60	100
								Total	**31**				

Basic Science Course (BS)													
S. No	**Course Code**	**Course Name**	**CAT**	**CT**	**Period / Week**						**Maximum Marks**		
					L	**T**	**P**	**S**	**C**	**TCP**	**CIA**	**ESE**	**Total**
1	P26VDPC11	Graph Theory and Optimization Techniques	PC	T	3	1	0	3	4	4	40	60	100

Professional Elective List (PE) SEMESTER II, ELECTIVE I													
S. No	**Course Code**	**Course Name**	**CAT**	**CT**	**Period / Week**						**Maximum Marks**		
					L	**T**	**P**	**S**	**C**	**TCP**	**CIA**	**ESE**	**Total**
1	P26VDPE01	PCB Circuit Design	PE	T	3	0	0	-	3	3	40	60	100
2	P26VDPE02	ASIC Design	PE	T	3	0	0	-	3	3	40	60	100
3	P26VDPE03	Embedded Systems Design	PE	T	3	0	0	-	3	3	40	60	100
4	P26VDPE04	FPGA Design Architectures	PE	T	3	0	0	-	3	3	40	60	100
5	P26VDPE05	Medical Image Systems	PE	T	3	0	0	-	3	3	40	60	100
6	P26VDPE06	Advanced Wireless Sensor Network	PE	T	3	0	0	-	3	3	40	60	100

Professional Elective List (PE) SEMESTER II, ELECTIVE II													
S. No	**Course Code**	**Course Name**	**CAT**	**CT**	**Period / Week**						**Maximum Marks**		
					L	**T**	**P**	**S**	**C**	**TCP**	**CIA**	**ESE**	**Total**
1	P26VDPE07	Advanced Digital Image Processing	PE	T	3	0	0	-	3	3	40	60	100
2	P26VDPE08	Soft Computing and Optimization Techniques	PE	T	3	0	0	-	3	3	40	60	100
3	P26VDPE09	MEMS and NEMS	PE	T	3	0	0	-	3	3	40	60	100
4	P26VDPE10	Testing and Testability of VLSI Circuits	PE	T	3	0	0	-	3	3	40	60	100
5	P26VDPE11	CAD for VLSI Circuits & Physical Design	PE	T	3	0	0	-	3	3	40	60	100
6	P26VDPE12	RF System Design	PE	T	3	0	0	-	3	3	40	60	100

Professional Elective List (PE)

SEMESTER III, ELECTIVE III

S. No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1	P26VDPE13	Robotics and Intelligent Systems	PE	T	3	0	0	-	3	3	40	60	100
2	P26VDPE14	DSP Structures for VLSI	PE	T	3	0	0	-	3	3	40	60	100
3	P26VDPE15	Nanotechnology	PE	T	3	0	0	-	3	3	40	60	100
4	P26VDPE16	Network on Chip	PE	T	3	0	0	-	3	3	40	60	100
5	P26VDPE17	Pattern Recognition	PE	T	3	0	0	-	3	3	40	60	100
6	P26VDPE18	Signal Integrity for High Speed Design	PE	T	3	0	0	-	3	3	40	60	100

Professional Elective List (PE)
SEMESTER III, ELECTIVE IV

S. No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1	P26VDPE19	VLSI for Wireless Communication	PE	T	3	0	0	-	3	3	40	60	100
2	P26VDPE20	VLSI Design and FPGA Implementation for Drone Systems	PE	T	3	0	0	-	3	3	40	60	100
3	P26VDPE21	Machine Learning in VLSI Design	PE	T	3	0	0	-	3	3	40	60	100
4	P26VDPE22	VLSI Design for Electric Vehicle Systems	PE	T	3	0	0	-	3	3	40	60	100
5	P26VDPE23	VLSI Architectures for Image Processing	PE	T	3	0	0	-	3	3	40	60	100
6	P26VDPE24	Advanced Transistor Modelling	PE	T	3	0	0	-	3	3	40	60	100

MANDATORY COURSE-I														
S.No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1.	P26MXMC01	English for Research Paper Writing	MC	T	2	0	0	-	0	2	100	-	100
2.	P26MXMC02	Gender Equity Program	MC	T	2	0	0	-	0	2	100	-	100
3.	P26MXMC03	Constitution of India	MC	T	2	0	0	-	0	2	100	-	100
MANDATORY COURSE-II													
4.	P26MXMC04	Technical Communication	MC	T	2	0	0	-	0	2	100	-	100
5.	P26MXMC05	Research and Publication Ethics	MC	T	2	0	0	-	0	2	100	-	100
6.	P26MXMC06	Disaster and Risk Management	MC	T	2	0	0	-	0	2	100	-	100

COMPETENCY ENHANCEMENT													
S.No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1.	P26VDEE01	Technical Seminar	EE	L	0	0	2	-	1	2	100	-	100
2.	P26VDEE02	Research Paper Review and Presentation	EE	L	0	0	2	-	1	2	100	-	100

SKILL DEVELOPMENT COURSE													
S.No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1.	P26VDSD21	Industry Oriented Course	SD (IOC)	LIT	1	0	2	-	2	3	100	-	100
2.	P26VDSD21	Mini Project	SD	L	0	0	2	-	2	2	100	-	100
3.	P26VDSD03	Project Work - Phase I	SD	L	0	0	12	-	6	12	100	-	100
4.	P26VDSD04	Project Work - Phase II	SD	L	0	0	24	0	12	24	60	40	100

Emerging Technology Elective (ET)													
S.No	Course Code	Course Name	CAT	CT	Period / Week						Maximum Marks		
					L	T	P	S	C	TCP	CIA	ESE	Total
1.	P26VDET01	Machine Learning for Automation	ET	T	3	0	0	-	3	3	40	60	100
2.	P26VDET02	Industrial Internet of Things 4.0	ET	T	3	0	0	-	3	3	40	60	100
3.	P26VDET03	VLSI Design for AI and Machine Learning	ET	T	3	0	0	-	3	3	40	60	100
4.	P26VDET04	Embedded Automation	ET	T	3	0	0	-	3	3	40	60	100
5.	P26VDET05	Advanced Physical Design and Optimization	ET	T	3	0	0	-	3	3	40	60	100
6.	P26VDET06	Quantum Technology	ET	T	3	0	0	-	3	3	40	60	100