Shree Sathyam
College of Engineering and Technology
Approved by AICTE, New Delhi & Affiliated to Anna University, Chennai.
NH-544, Salem - Coimbatore Highways, Kuppanur, Sankari Taluk, Salem - 637301, TamilNadu, India.
Email : principal@shreesathyam.edu.in Web : www.shreesathyam.edu.in Phone : 04283 - 244080

Department of Electronics and Communication Engineering

EC3552 VLSI and Chip Design

Unit 5 – Introduction to wafer to chip fabrication process flow, Microchip design process & issues in test and verification of complex chips

Presented by
Mr. A. Saravanamoorthy, M.E.,
Assistant Professor

Date: 27.10.2023 & Time: 2.35 PM (6th Hour)

MATERIAL PREPARATION

Purification of Silicon

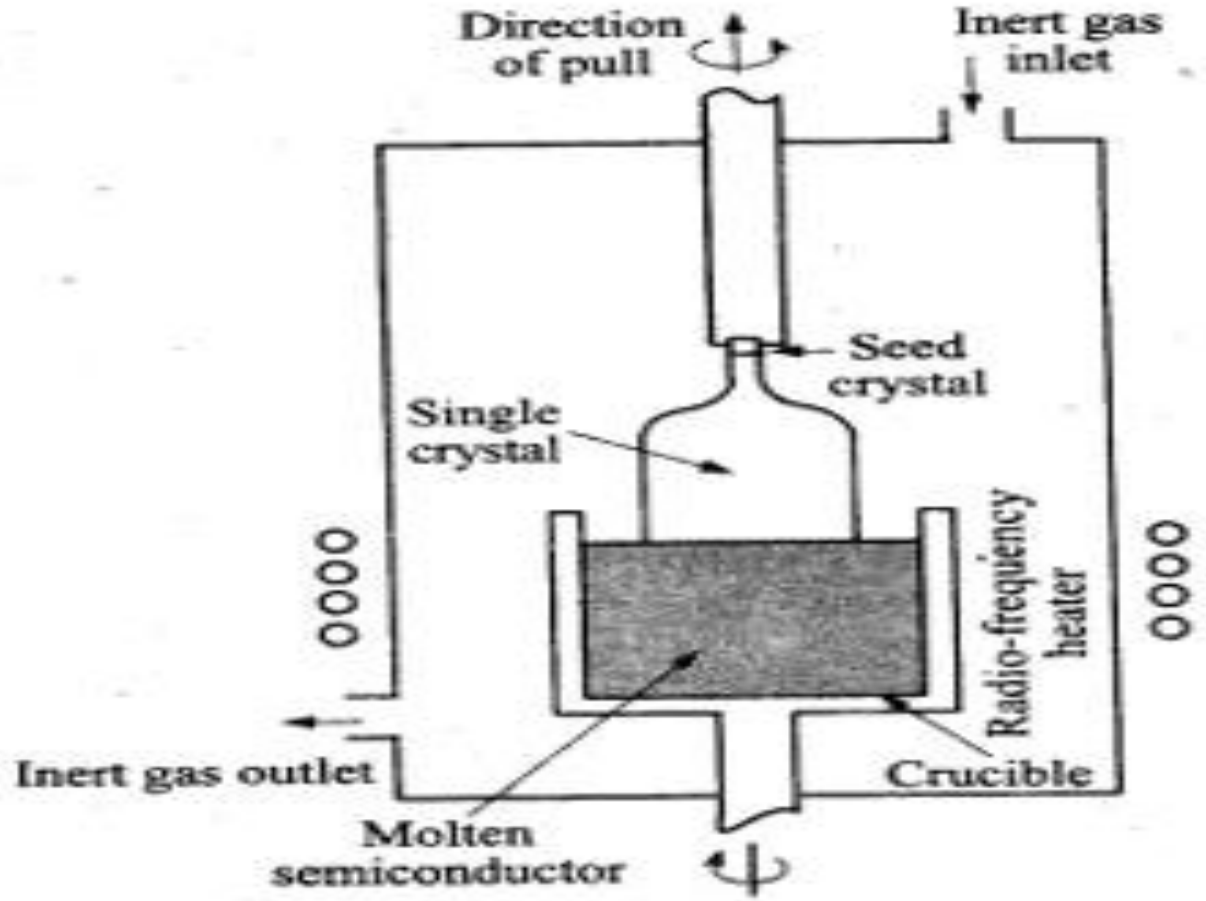
Silicon is abundantly available in nature in the form of SiO_2 (sand) which forms about 20% of earth's crust. Metallurgical Grade Silicon (MGS) is obtained by reduction of quartzite (a crystalline form of SiO_2 available in the form of rock) in a carbon arc furnace. From MGS Electronic Grade Silicon (EGS) is obtained by distillation process. EGS is polycrystalline in nature. It consists of impurities of the order of 1 ppb. (1 unwanted impurity per 1 billion or 10^9 silicon atoms).

Crystal Growth

This process is done to convert polycrystalline silicon to single crystalline silicon Crystallisation takes place if molten silicon is allowed to solidify to a seed crystal. (Seed crystal is a highly pure single crystalline silicon which is used as the starting material for crystal growth). Two established processes used for crystal growth are:

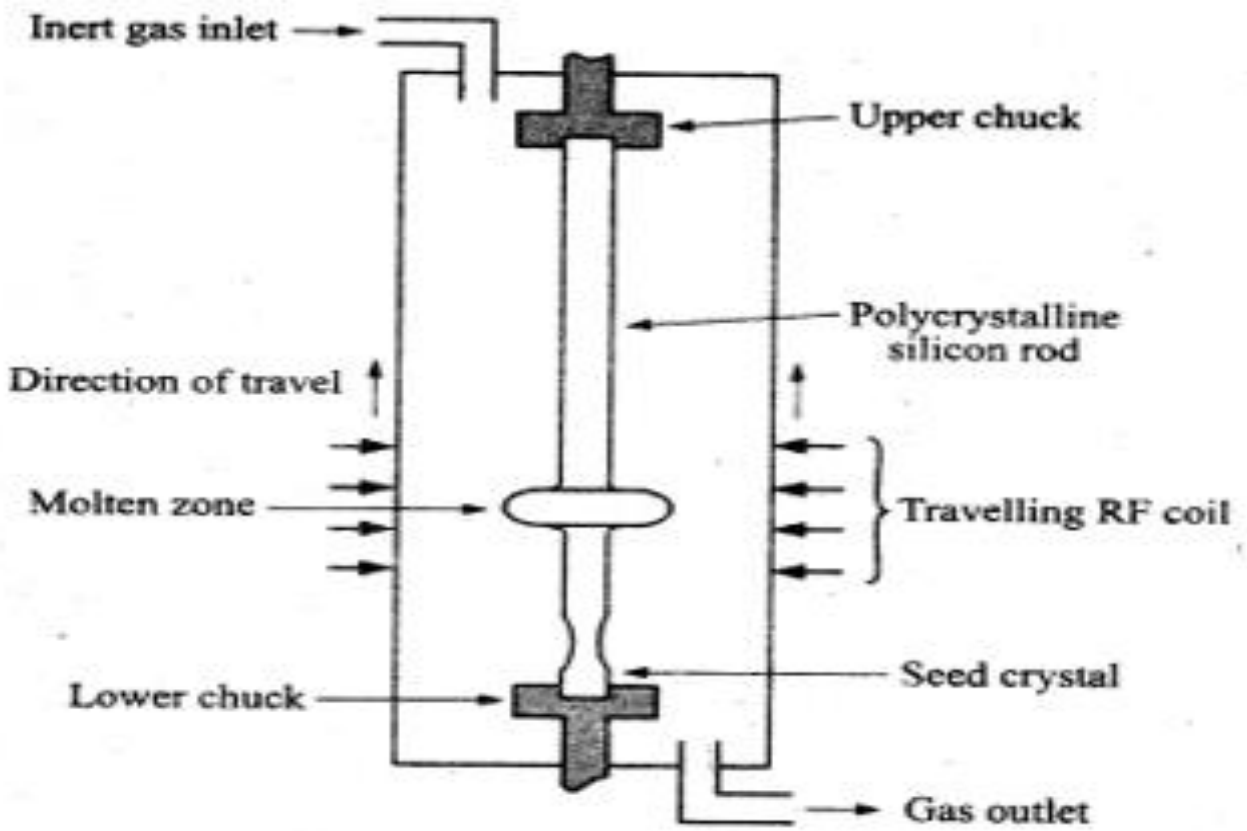
(1) Czochralski growth (CZ process) and
(2) Float zone process (FZ process)

Czochralski growth (CZ process)



Date: 27.10.2023 & Time: 2.35 PM (6th Hour)

Float zone process (FZ process)



Crystal Slicing and Wafer Preparation

The crystal ingot has diameter upto 12 inches and length of 100 cm. This ingot is ground to an exactly cylindrical shape. A flat is ground at the end of the bar. A slice is cut from this end and the crystal orientation is determined by X-ray diffraction method. The slicing, is done at different angles until the desired orientation of the crystal at the surface is obtained.

The crystal is then cut into slices called wafers. Thickness of wafers vary from 0.4 to 1mm. The slicing is done by a ring shaped saw blade made of stainless steel. Diamond is bonded on the inner rim of the saw and cutting process is water cooled. About one third of the material is lost as saw dust.

The sliced crystal is subjected to two sided lapping under pressure with a mixture of Al_2O_3 and glycerine. Then, the wafers are subjected to chemical etching in mixture of HF, HNO_3 and acetic acid. One side of the wafer is then polished to mirror finish. Devices are fabricated on this wafer. Processing are done on the polished surface.

FABRICATION PROCESSES

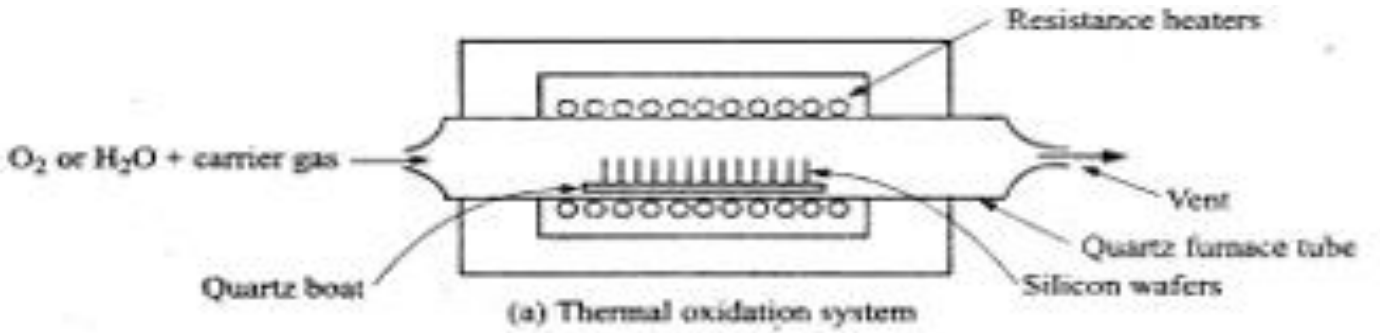
The important unit processes involved in the fabrication of devices are

1. Oxidation
2. Diffusion
3. Ion implantation
4. Epitaxy
5. Isolation
6. Lithography
7. Metallization

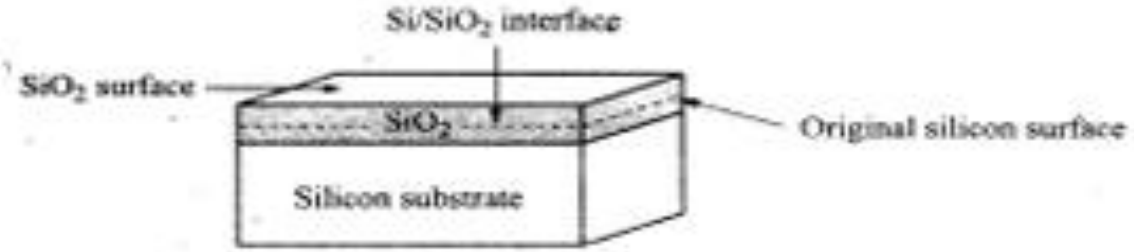
The basic integrated circuit fabrication process is known as planar process in which introduction of impurities and metallic connections arc carried out from the top surface of the wafer. In planar process, several wafers consisting of similar devices or circuits can be processed simultaneously. Precise control of temperature, humidity and extremely clean environment are required for fabrication of devices.

Thermal Oxidation

$$Si + O_2 \rightarrow SiO_2 \text{ (dry oxidation)}$$
$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \uparrow \text{ (wet oxidation)}$$

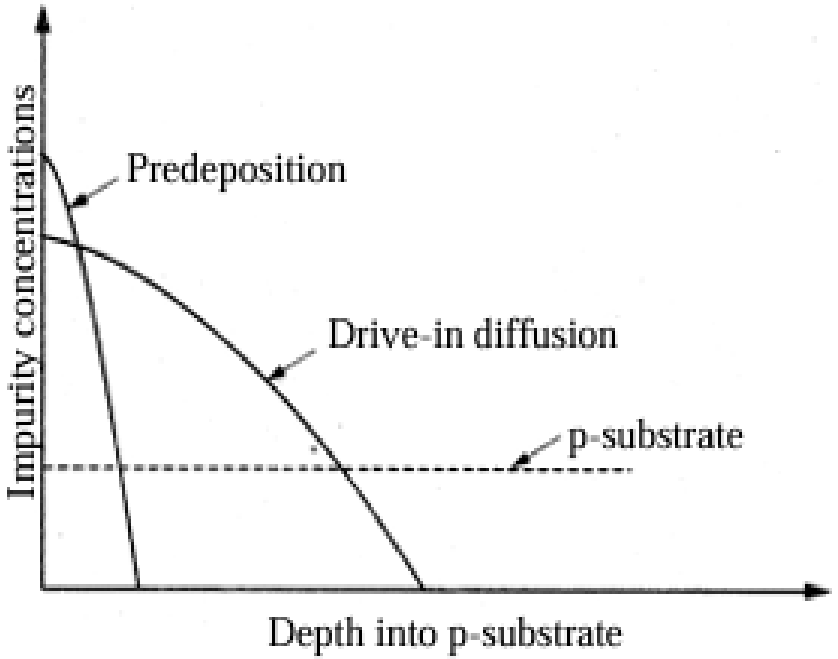


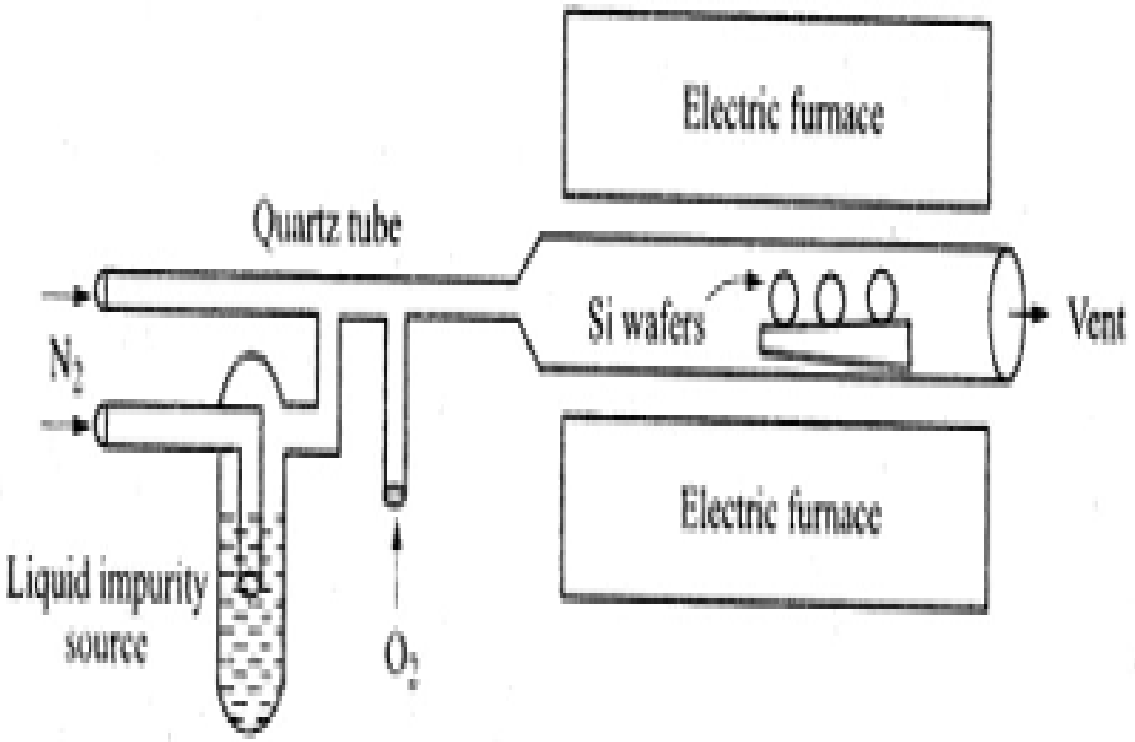
(a) Thermal oxidation system



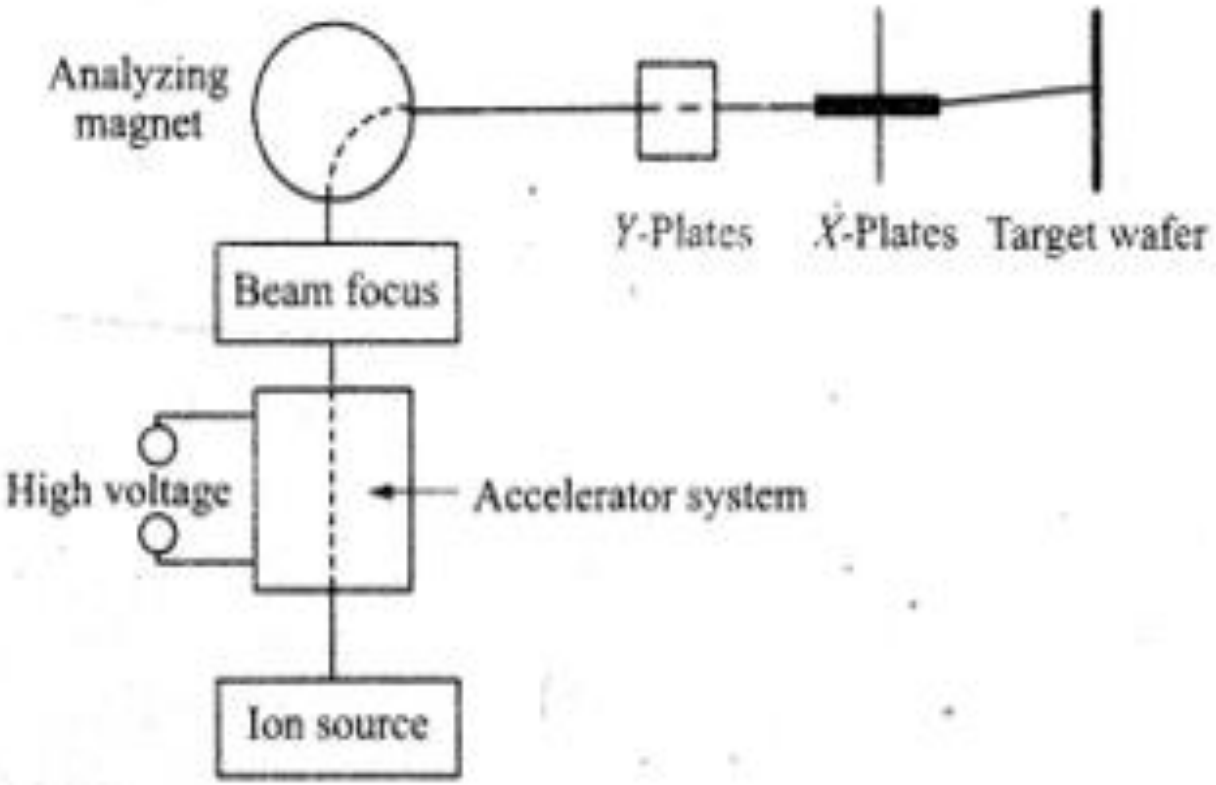
(b) Oxide grown silicon

Diffusion

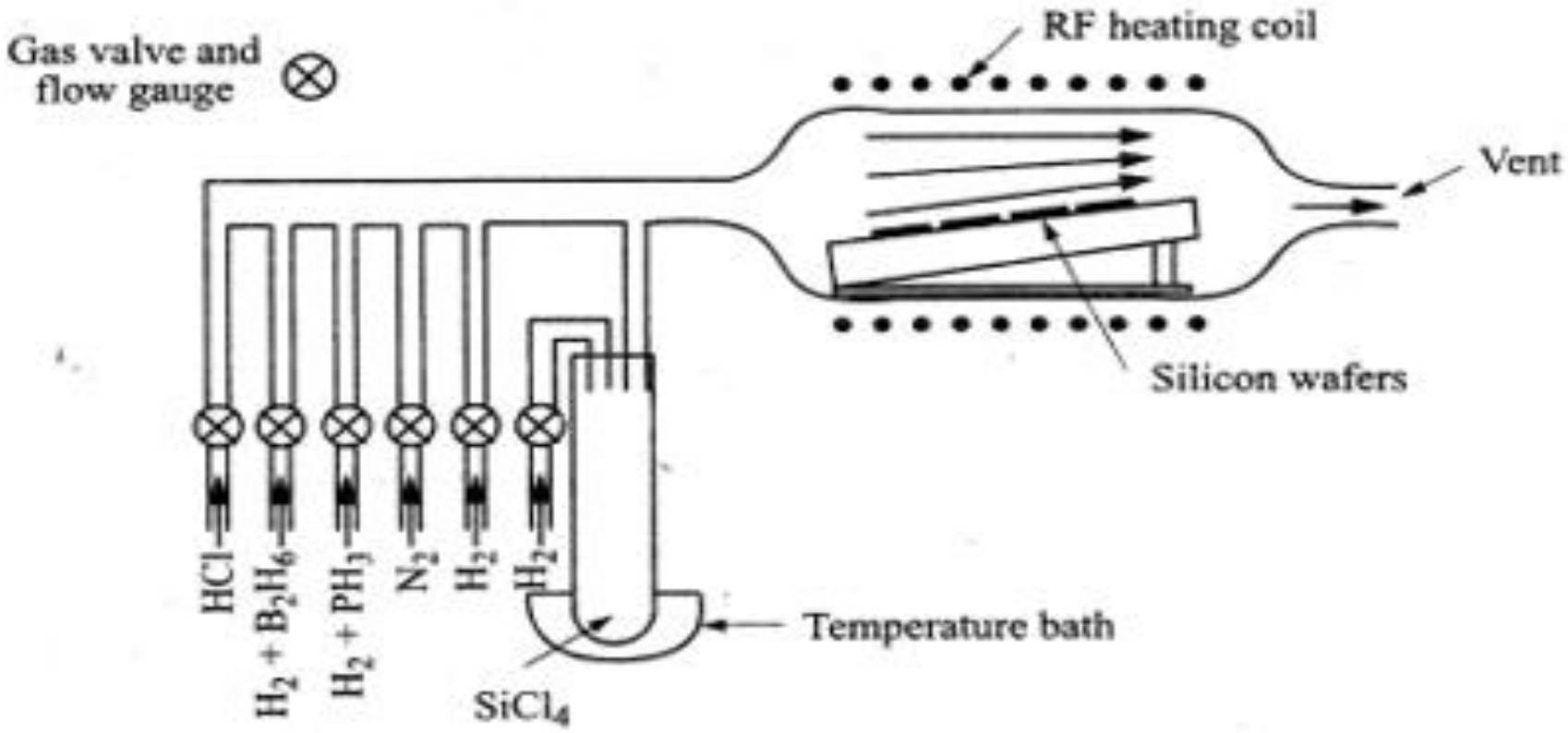

Impurity concentrations
Predeposition
Drive-in diffusion
p-substrate
Depth into p-substrate


Electric furnace
Quartz tube
Si wafers
Vent
N_2
Electric furnace
Liquid impurity source
O_2

Ion Implantation



Epitaxial Growth



Other Deposited Layers

a. Deposited Oxide Layers

If silicon surface is covered with other layers, oxide must be deposited by chemical vapour deposition (CVD) process. There are number of options available for the reactive components. A mixture of silane and oxygen at 450° C may be used as the reactive component for deposition of a layer of SiO_2.

$$SiH_4 + 2O_2 \rightarrow SiO_2 + 2H_2O$$

b. Nitride Layers

Nitride layer finds use as an oxidation mask, high permittivity layer for capacitor structures, passivation layer against moisture and sodium ions, etc. Nitride layer can be deposited by CVD of ammonia with silane in the temperature range of 700-1000° C.

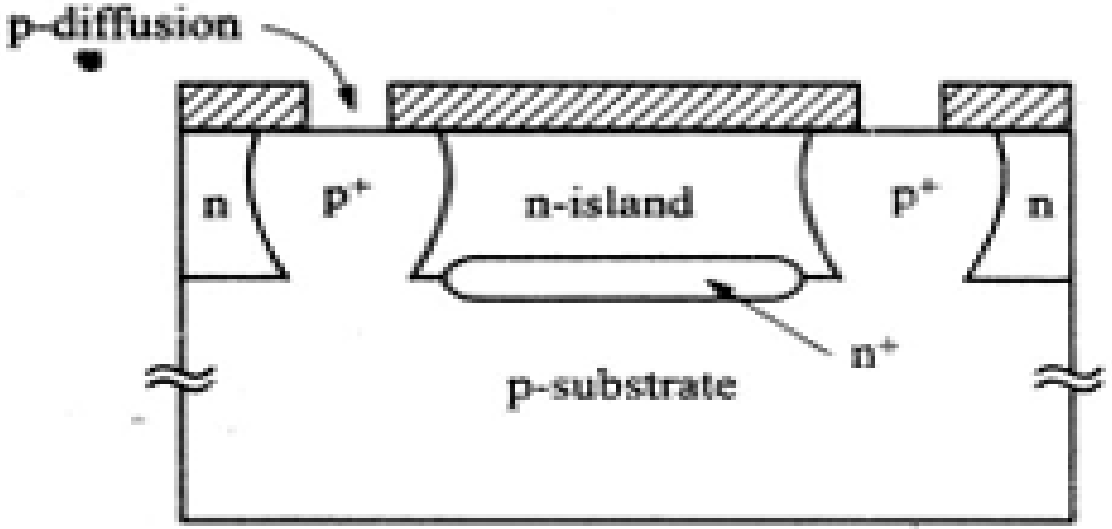
$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \uparrow$$

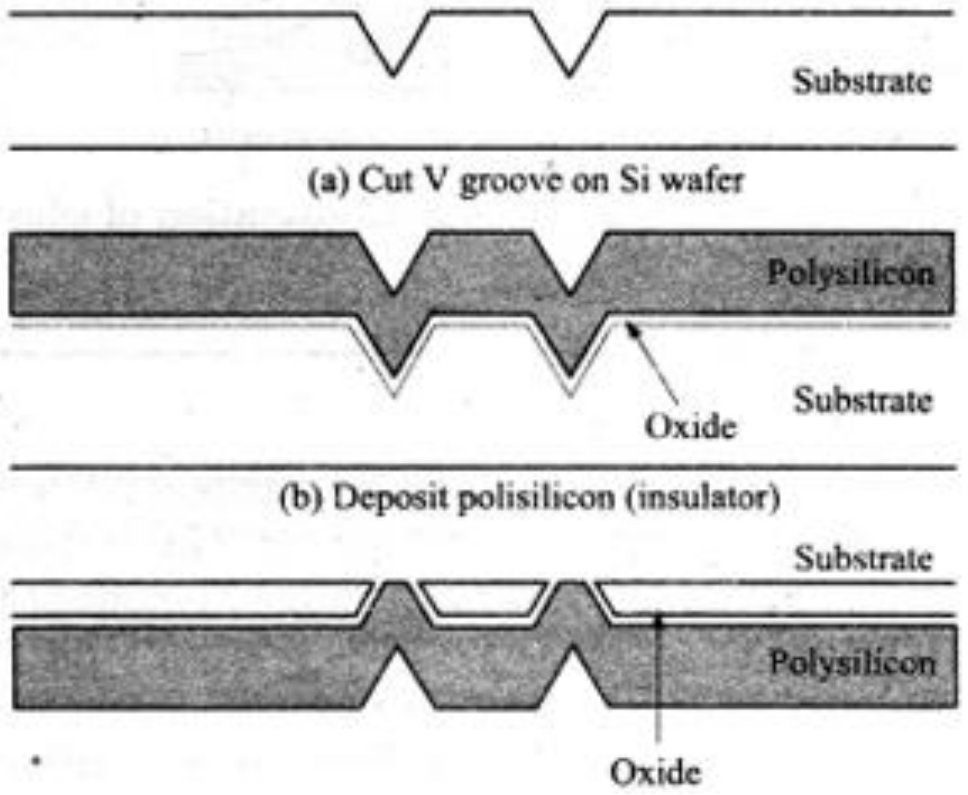
c. Polycrystalline Silicon

Polycrystalline silicon (or polysilicon) finds use as a substitute for epitaxial layer when the silicon surface is covered by another layer (metal or oxide). Heavily doped polysilicon is used as an interconnect material in multilevel metallization. It is also used for passivation, in undoped form. Added oxygen increases the resistivity further. Polysilicon is formed in a low pressure furnace at 600-650° C by pyrolysis of silane.

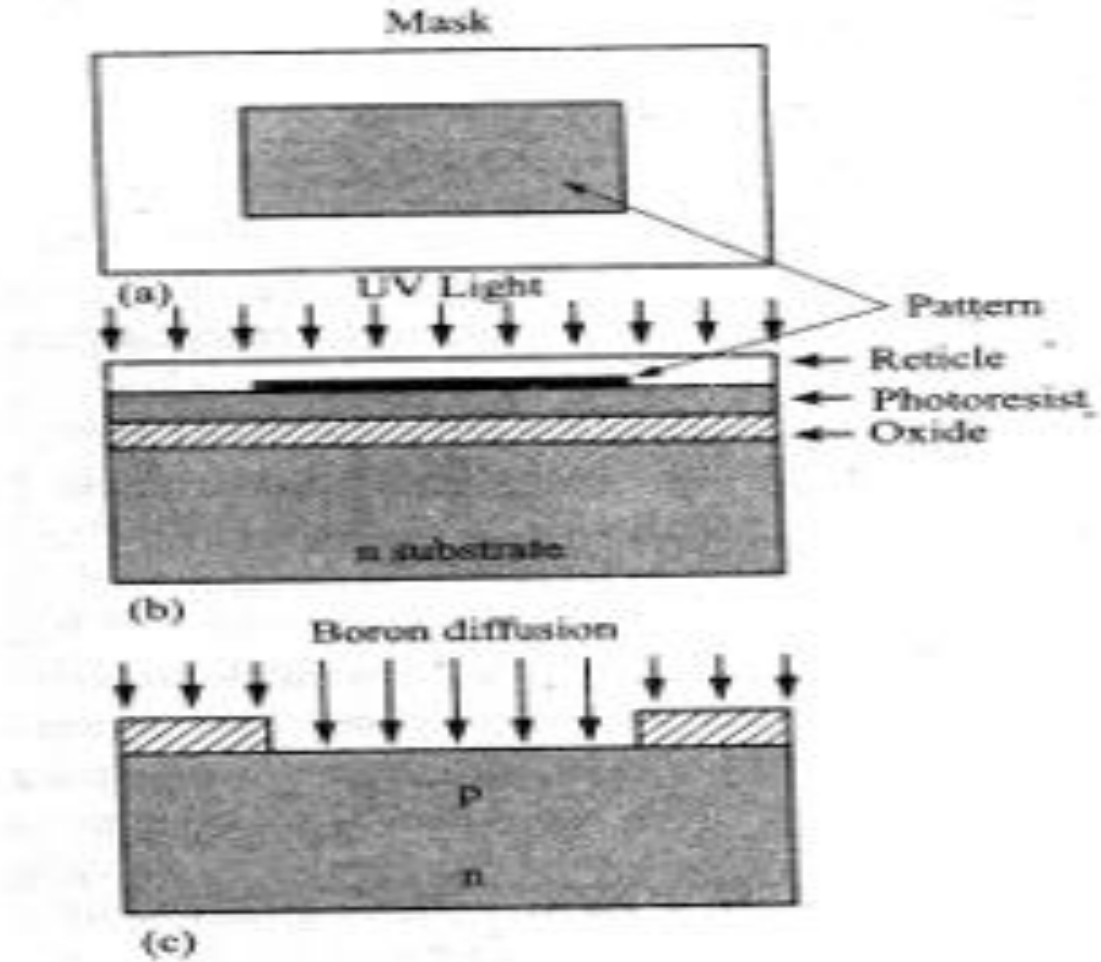
$$SiH_4 \rightarrow Si + 2H_2$$

Isolation


p-diffusion
n
p+
n-island
p+
n
n+
p-substrate


Substrate
(a) Cut V groove on Si wafer
Polysilicon
Oxide
Substrate
(b) Deposit polisilicon (insulator)
Substrate
Polysilicon
Oxide

Masking and Lithography



Pattern Definition

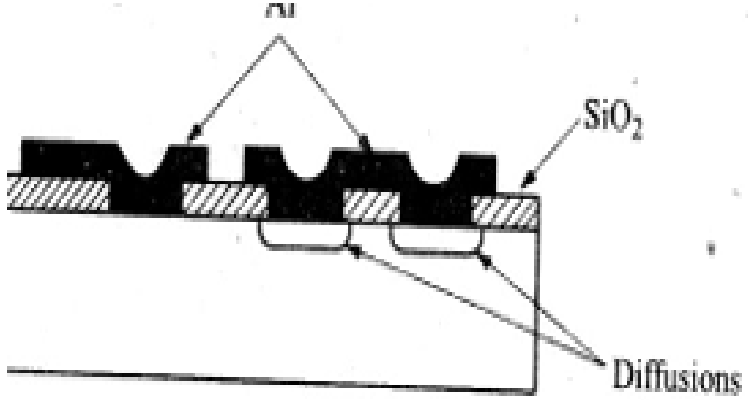
a) **Wet Etching**

b) **Plasma Etching**

c) **Reactive Ion Etching**

Metallisation and Interconnection

- **Resistance heating**
- **Electron beam heating**
- **Sputtering**



Microchip design process & issues in test and verification of complex chips

Definition

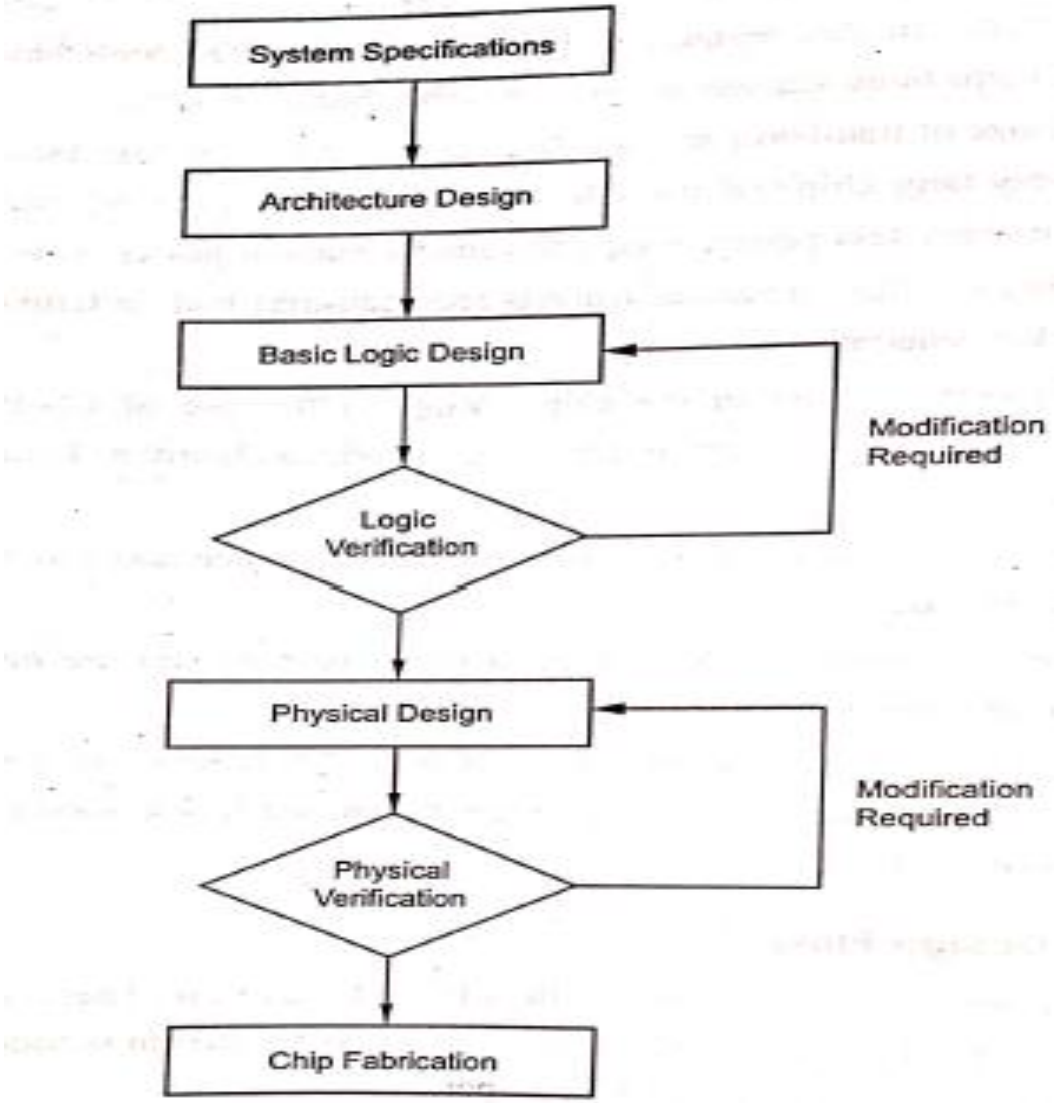
- *A microchip is also called a chip, computer chip* or *Integrated Circuit* (IC) *which is a unit of integrated circuitry that is manufactured at a microscopic scale using a semiconductor material, such as silicon or, to a lesser degree, germanium.*
- *Electronic components, such as transistors and resistors, are etched into the material in layers, along with intricate connections that link the components together and facilitate the flow of electric signals.*

- Microchip components are so small and are measured in nanometers ***(nm).*** Some components are now under 10 nm, making it possible to fit billions of components on a single chip.

Chip Design

- ***Chip design*** *is a process of designing a chip and is an essential part of electronics engineering. This process of chip design involves the knowledge of circuit design and its logic formation.*
- All chips are made using basic elements which are known as transistors. The *Metal Oxide Silicon Field Effect Transistor* (MOSFET) is the basic building block of digital chips which is used to make complex circuits.

Chip Design Flow



Date: 27.10.2023 & Time: 2.35 PM (6th Hour)

Issues in Test and Verification

(i) Specification Problems.
- Insufficient definition.
- Lack of necessary conditions.
- Misunderstandings between people.

(ii) Implementation Problems.
- Insufficient performance.
- Improper block partitioning.
- Block interface mismatching.
- Excessive power consumption.

(iii) Verification Problems.
- Slow software simulation.
- Problems with the hardware –software interface.
- System function verification.

References

1. Michael J Smith ,” Application Specific Integrated Circuits, Addison Wesley.

2. P. Rashinkar, Paterson and L. Singh, "System-on-a-Chip Verification-Methodology and Techniques", Kluwer Academic Publishers,2001